

# Compal Confidential

## Schematics Document

AUBURNDALE/CLARKSFIELD with  
Intel IBEX PEAK-M core logic

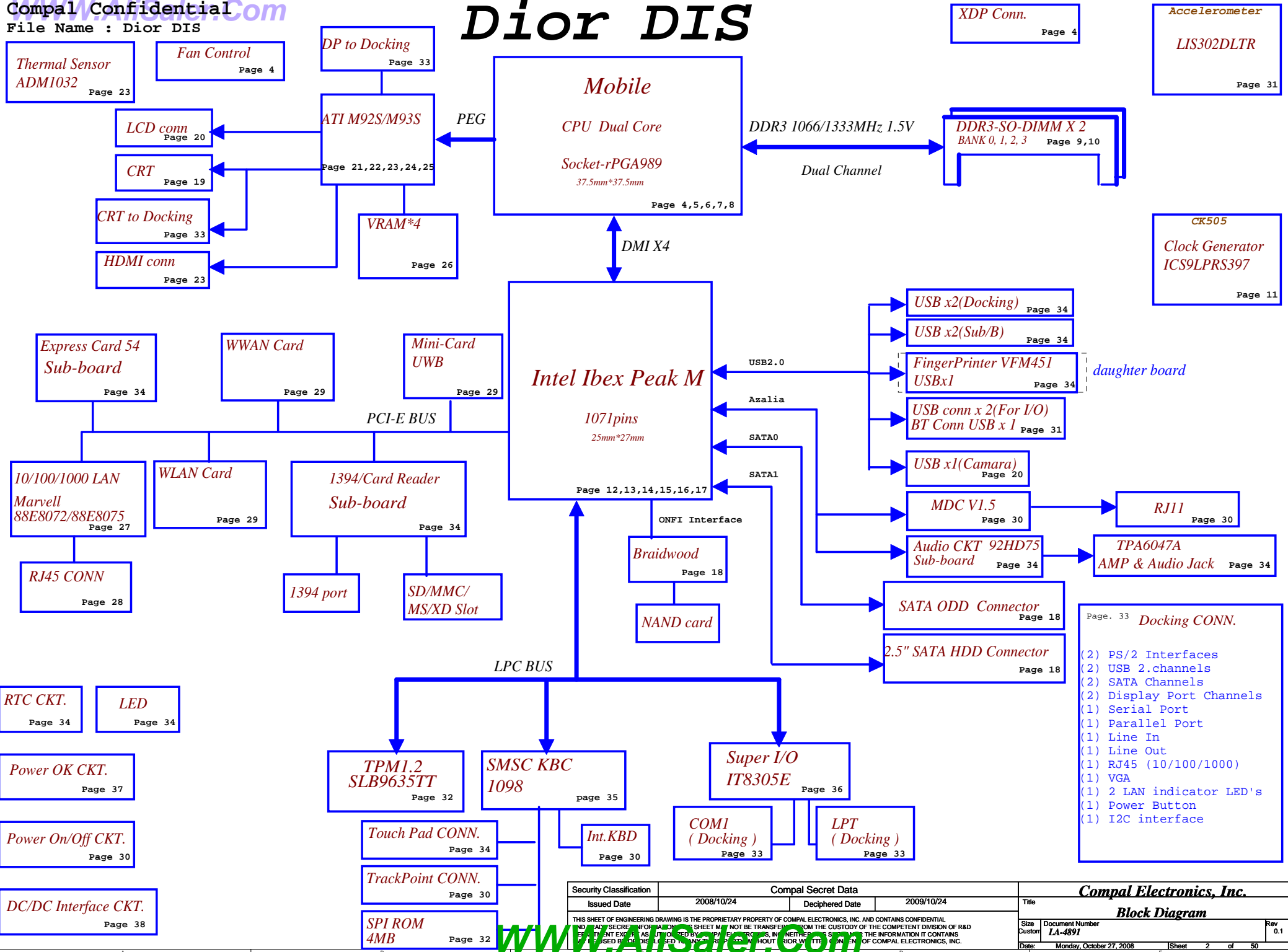
Dior DIS

2008-10-30

REV:0.1

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Issued Date	2008/10/24	Deciphered Date	2009/10/24	Title	
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				Custom	LA-4891
				Date:	Thursday, October 30, 2008
				Sheet	1 of 50
				Rev	0.1

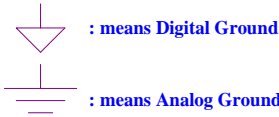
# Dior DIS



Voltage Rails ( O MEANS ON X MEANS OFF )

<div>power plane</div> <div>State</div>	+RTCVCC	+B +3VL	+5VALW +3VALW	+1.5V +0.75V	+5VS +3VS +1.5VS +NVVDD +VCCP +CPU_CORE +1.05VS +1.8VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

Symbol Note :



Install below 43 level BOM structure for ver. 0.1

- DEBUG@ : means just build when PCIE port 80 CARD function enable. Remove before MP
- M92@ : Install for M92 Graphic controller
- 8072@ : Install for 8072 NIC controller
- 1098@ : Install for 1098 KBC controller
- CK32@ : Install for 32 pin CLOCK GEN

Install below 45 level BOM structure for ver. 0.1

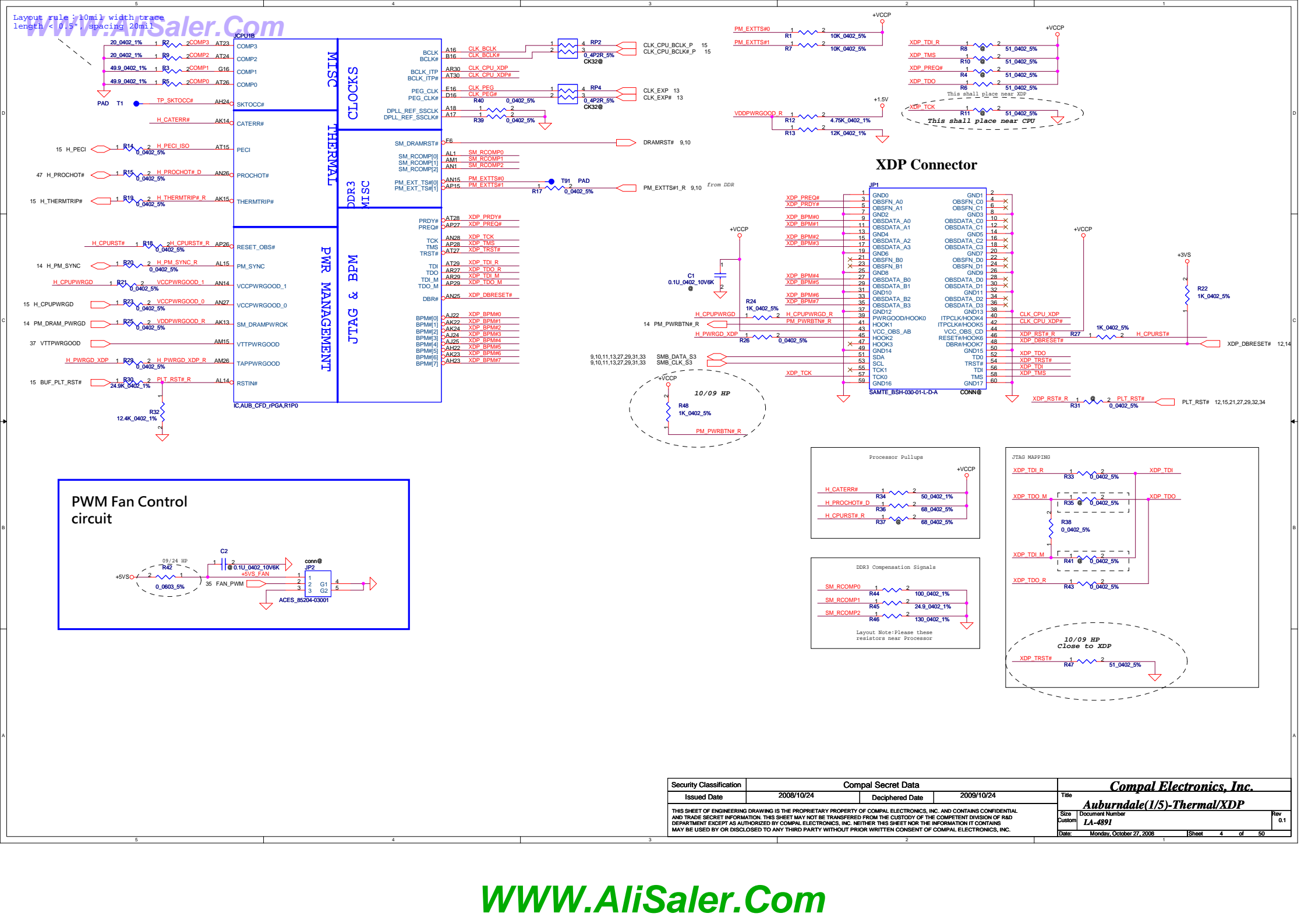
- 45@ : means just put it in the BOM of 45 level.

Reserve below BOM structure for ver. 0.1

- @ : means just reserve , no build
- CONN@ : means ME part.
- M93@ : Install for M93 Graphic controller
- 8075@ : Install for 8075 NIC controller
- 1091@ : Install for 1091 KBC controller
- CK72@ : Install for 72 pin CLOCK GEN

SMBUS Control Table

	SOURCE	BATT	XDP	SODIMM	CLK CHIP	MINI CARD	DOCK	NIC	THERMAL SENSOR	G-SENSOR
SMB_EC_CK1 SMB_EC_DA1	SMSC1098	V	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	Calpella	X	V	V	V	V	V	V	X	V
SML0CLK SML0DATA	Calpella	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	X	X	V	X



Layout rule : 10mil width trace  
length < 0.5" / spacing 20mil

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**Layout Rule:** 10mil width trace, length < 0.5", spacing 20mil

**Legend:**

- COMP3 AT23
- COMP2 AT24
- COMP1 G16
- COMP0 AT26
- SKTOCC# AH24
- CATERR# AK14
- PECI AT15
- PROCHOT# AN26
- THERMTRIP# AK15
- RESET\_OBS# AP26
- PM\_SYNC AL15
- VCCPWGOOD\_1 AN14
- VCCPWGOOD\_0 AN27
- SM\_DRAMPWROK AK13
- TAPPWGOOD AM15
- RSTIN# AL14
- IC\_AUB\_CFD\_PGA\_R1P0

**Processor Pullups**

- H\_CATERR# R34 50\_0402\_1%
- H\_PROCHOT#\_D R36 68\_0402\_5%
- H\_CPURST# R37 68\_0402\_5%

**DDR3 Compensation Signals**

- SM\_RCOMP0 R44 100\_0402\_1%
- SM\_RCOMP1 R45 249\_0402\_1%
- SM\_RCOMP2 R46 130\_0402\_1%

**JTAG Mapping**

- XDP\_TDI# R33 51\_0402\_5%
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- XDP\_TDO R6 51\_0402\_5%
- XDP\_TCK R11 51\_0402\_5%
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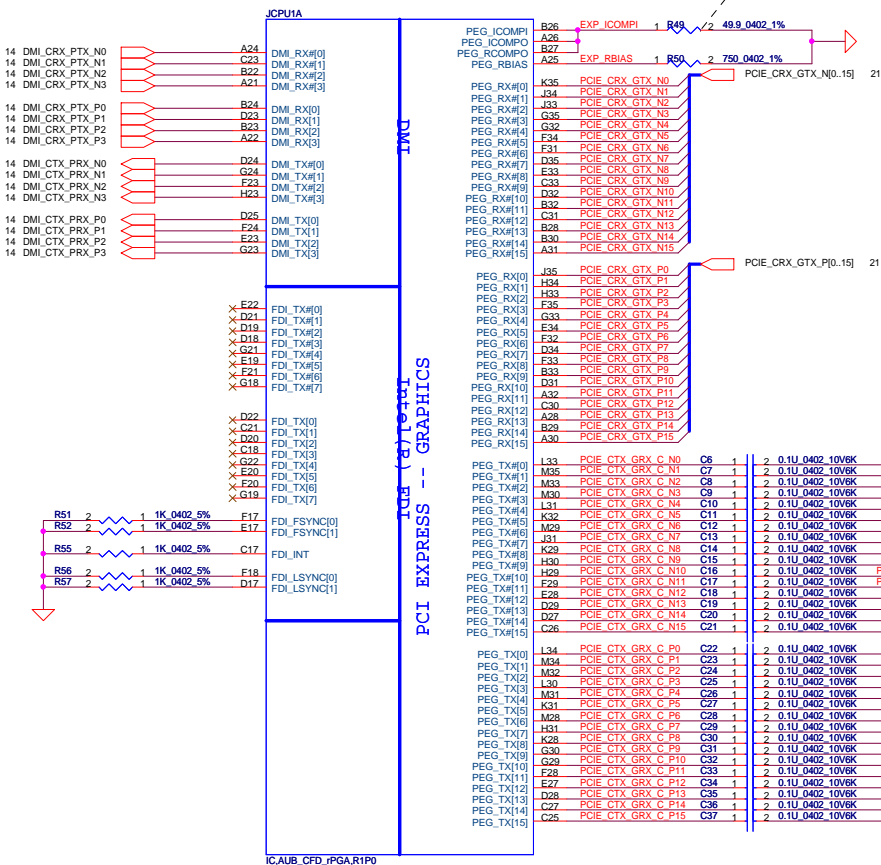
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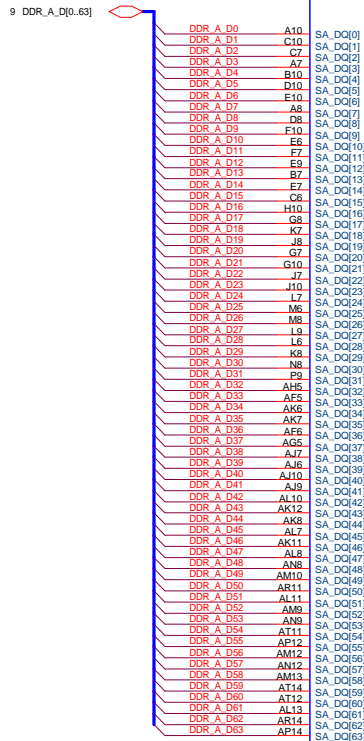


### CFG Straps for PROCESSOR

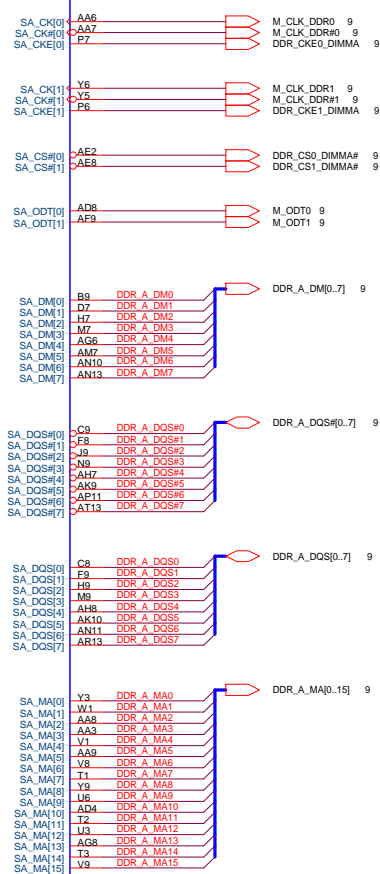
CFG0	1: Single PBG 0: Bifurcation enabled Not applicable for Clarkfield Processor
CFG3	1: Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, .....
CFG4	1: Disabled/ No Physical Display Port attached to Embedded Display Port 0: Enabled/ An external Display Port device is connected to the Embedded Display Port

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JCPUIC

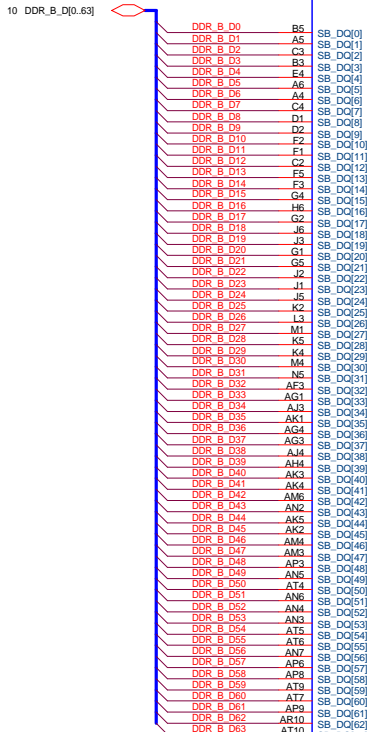


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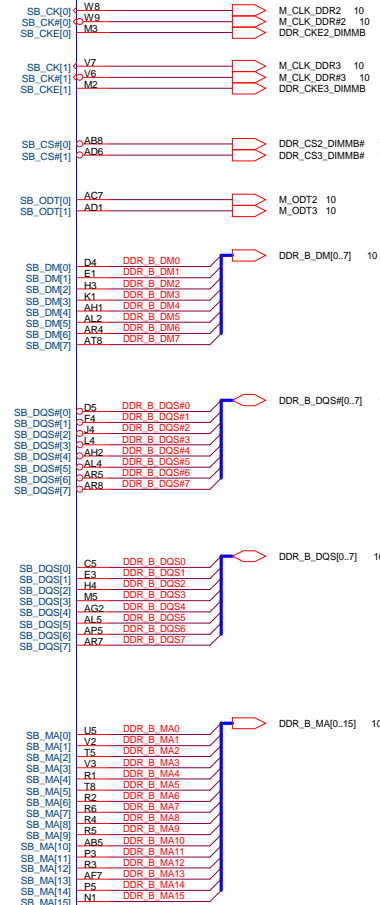


IC:AUB\_CFD\_rPGA,R1P0

JCPU1D



DDR SYSTEM MEMORY - B

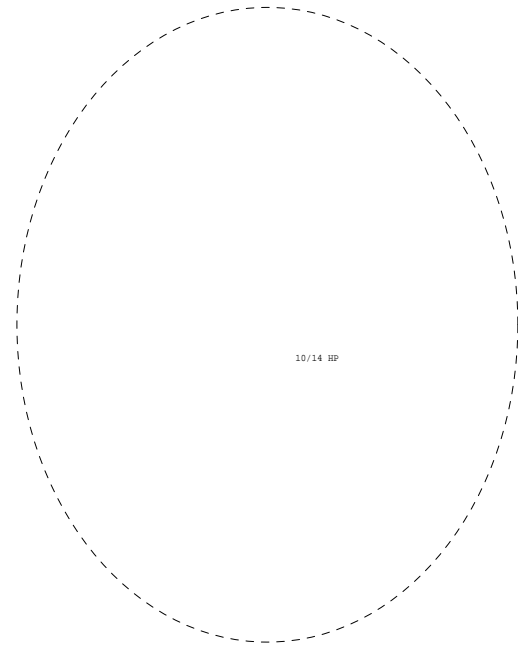
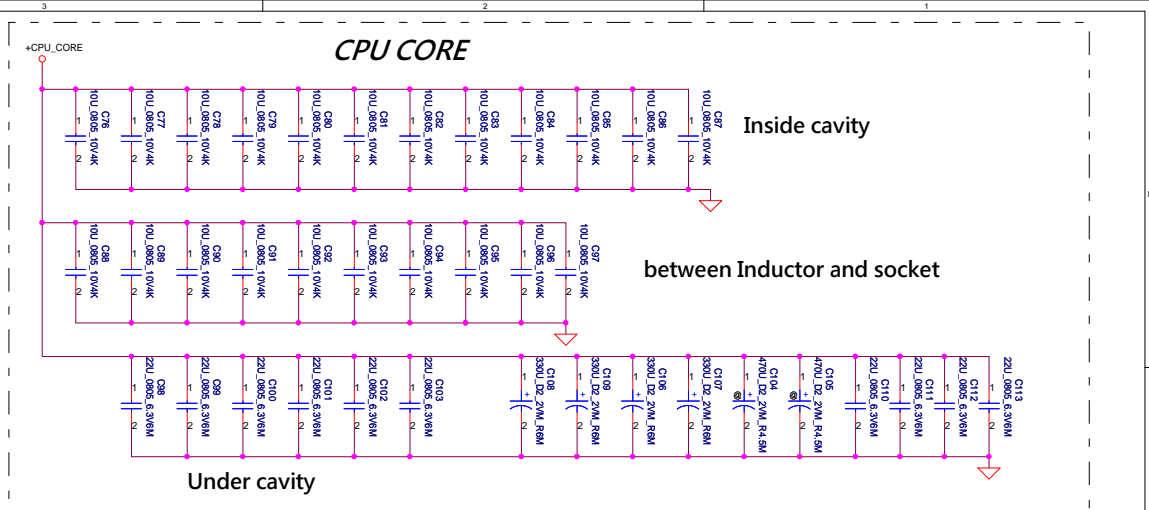
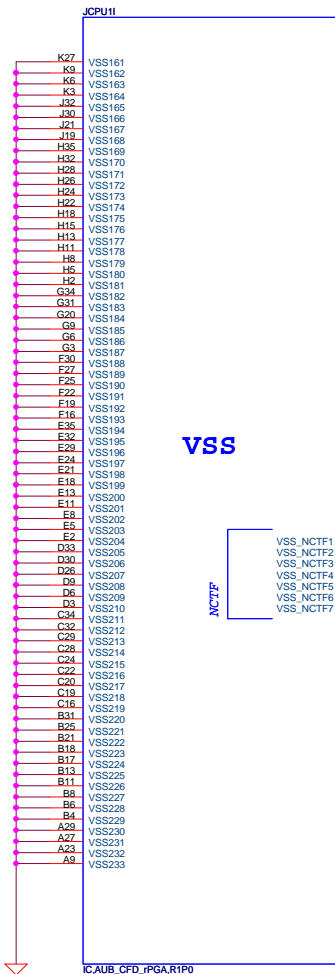
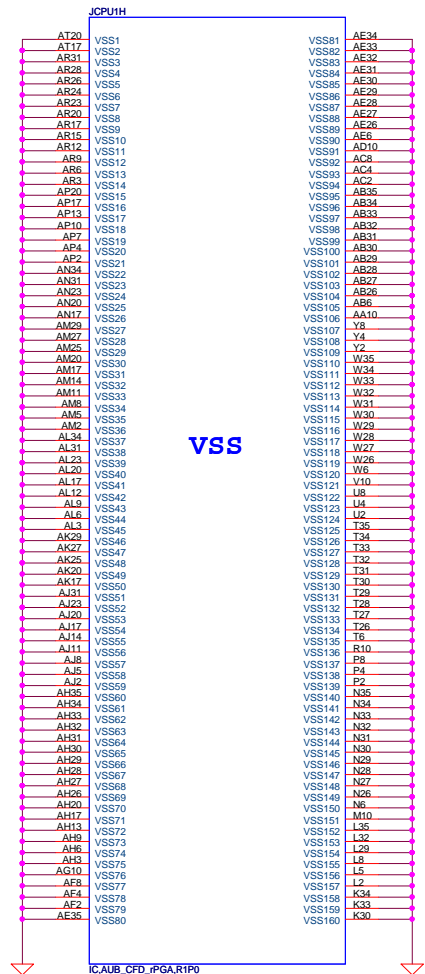


IC:AUB\_CFD\_rPGA,R1P0

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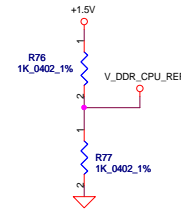




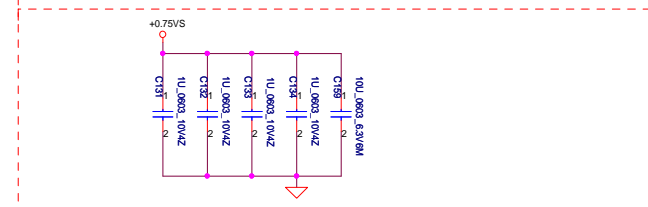
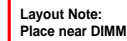
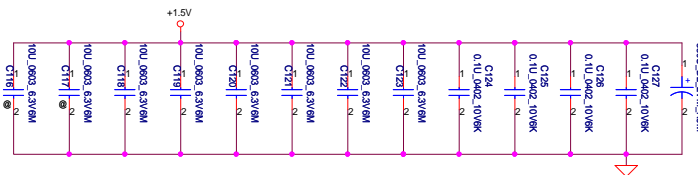
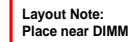


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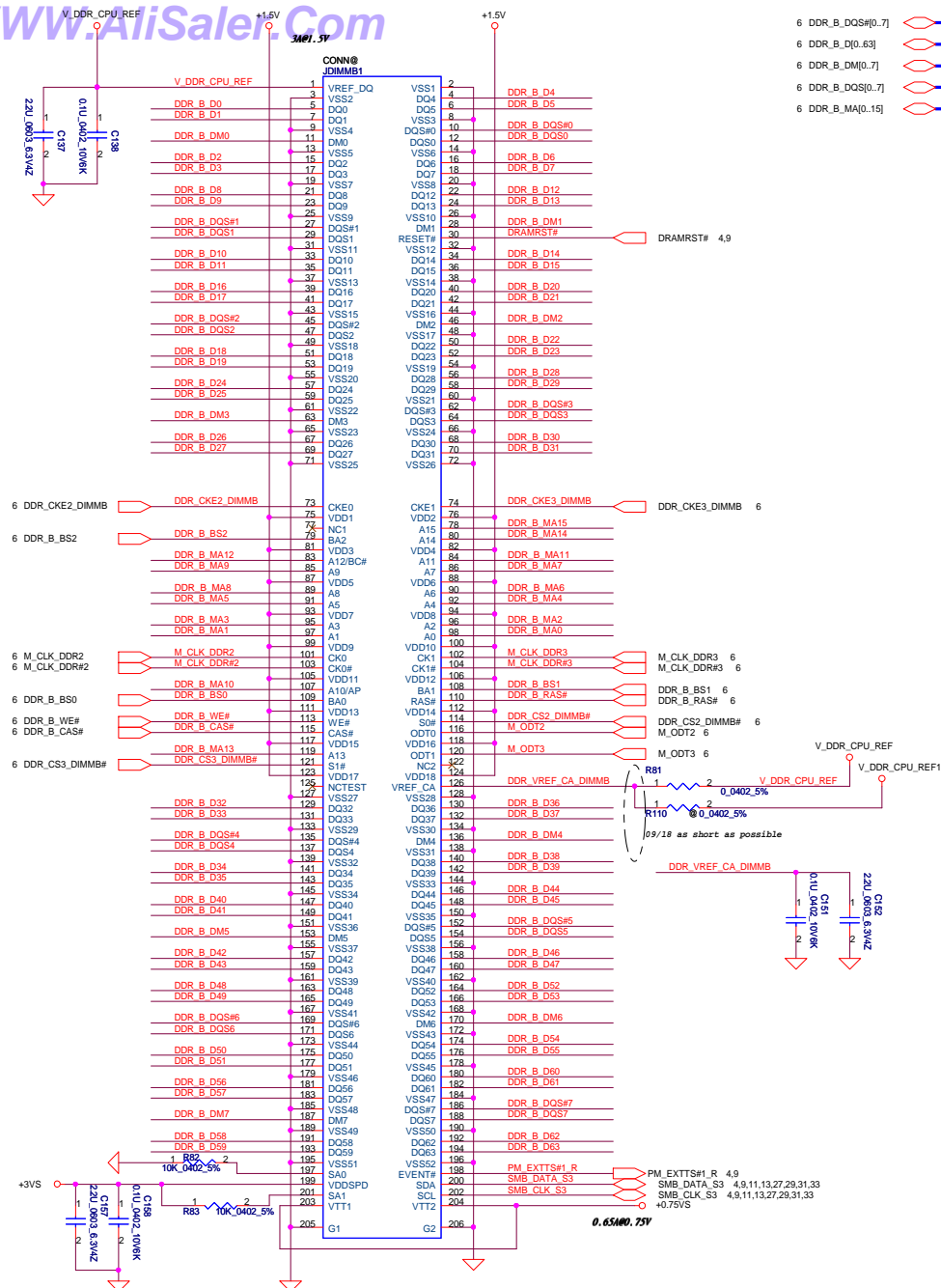




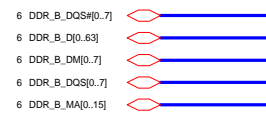
VREFDQ		
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M3	V_DDR_CPU_REF0	R104, R110
	V_DDR_CPU_REF1	



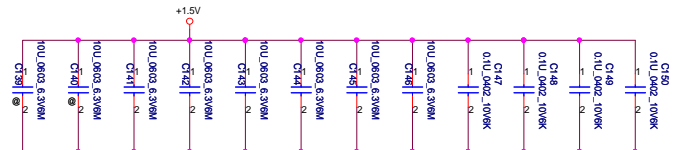
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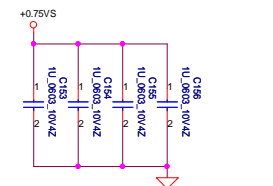
***BOT SLOT***



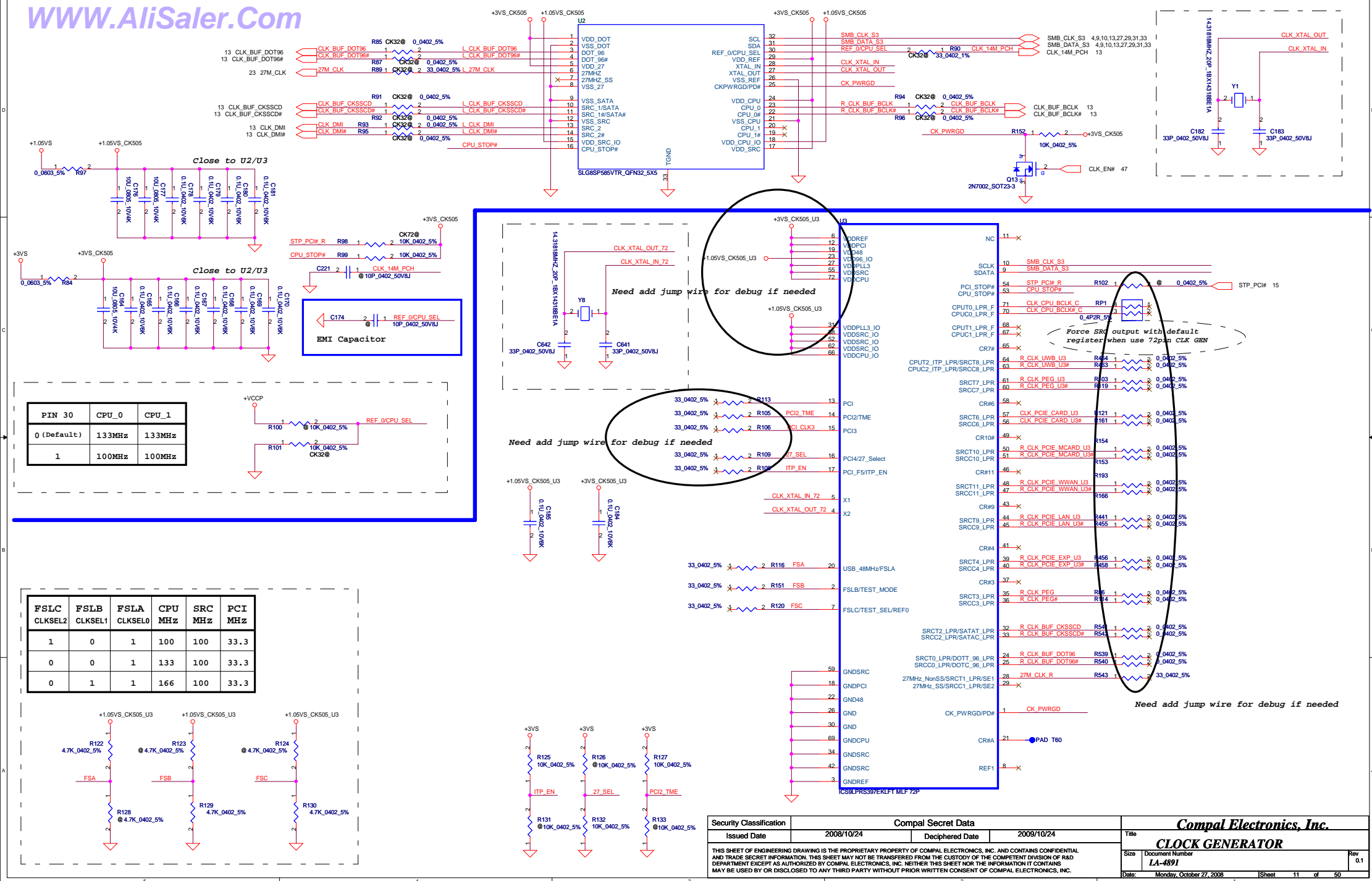
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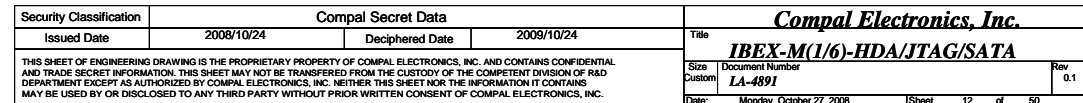


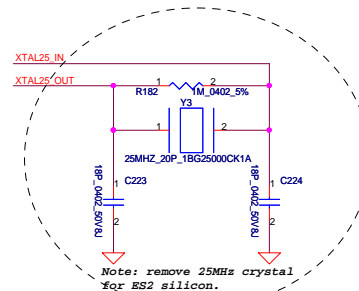
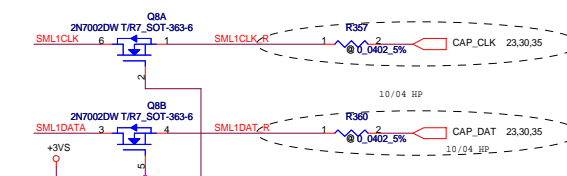
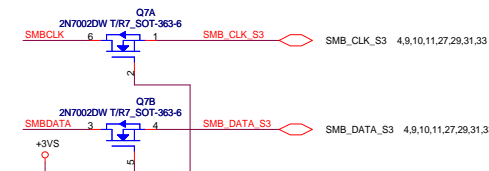
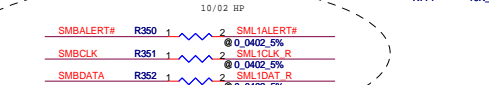
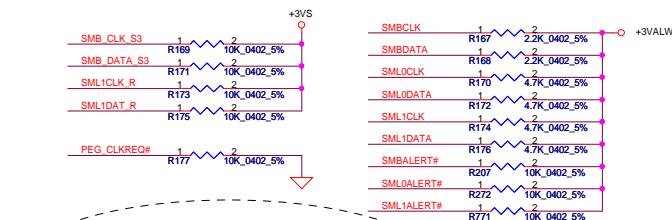
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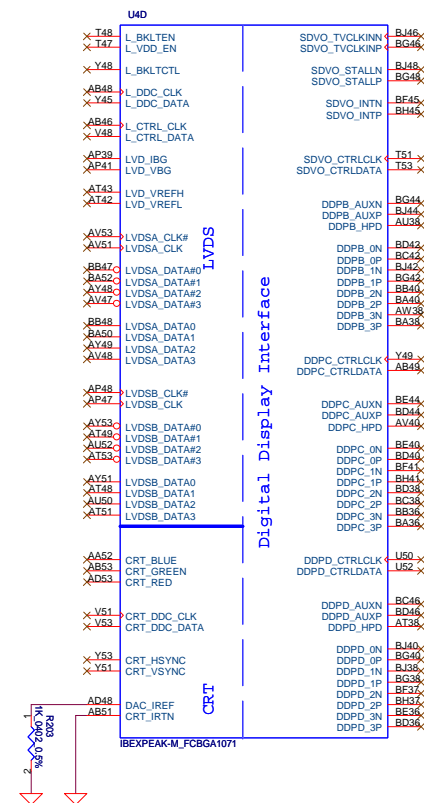
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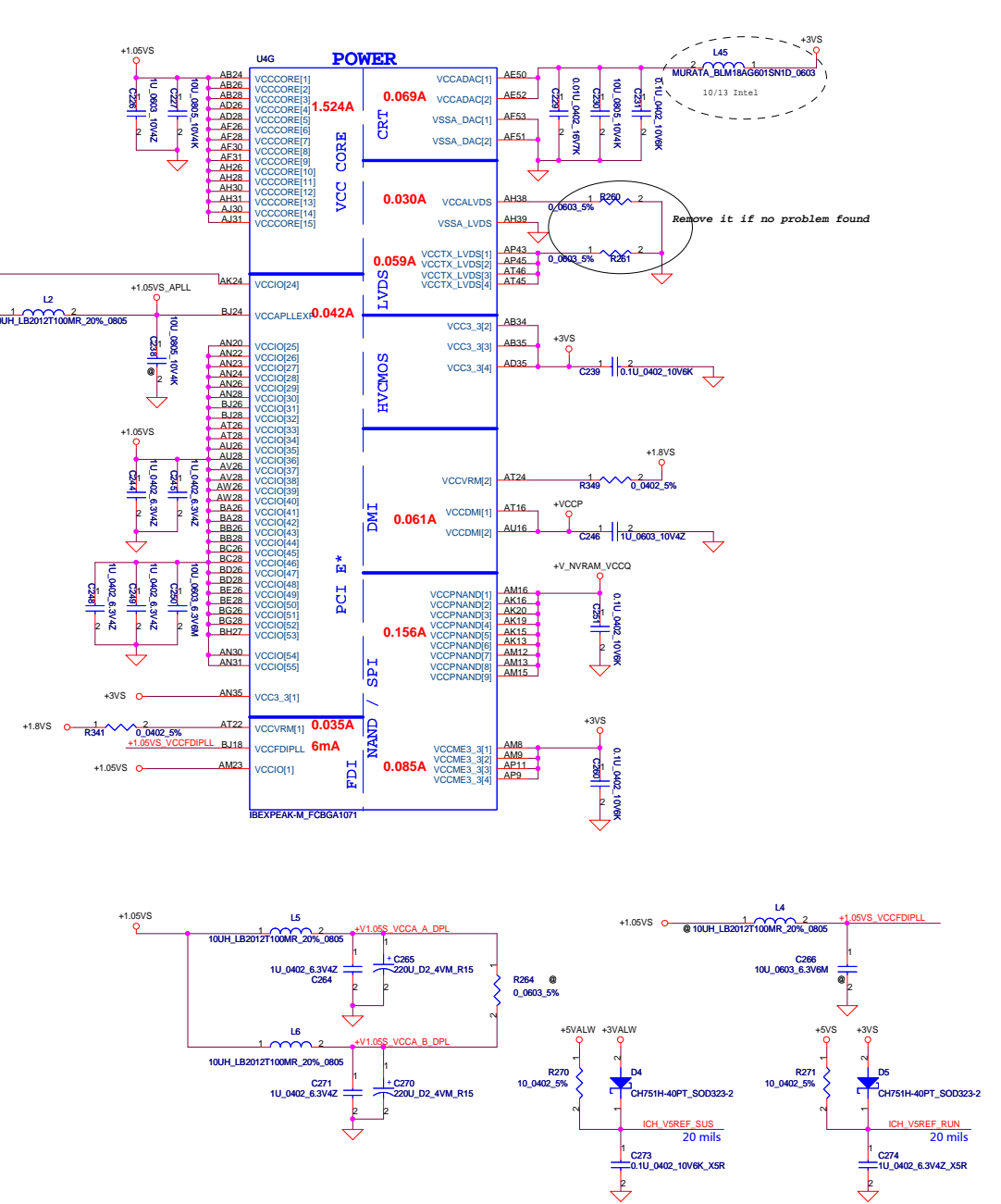
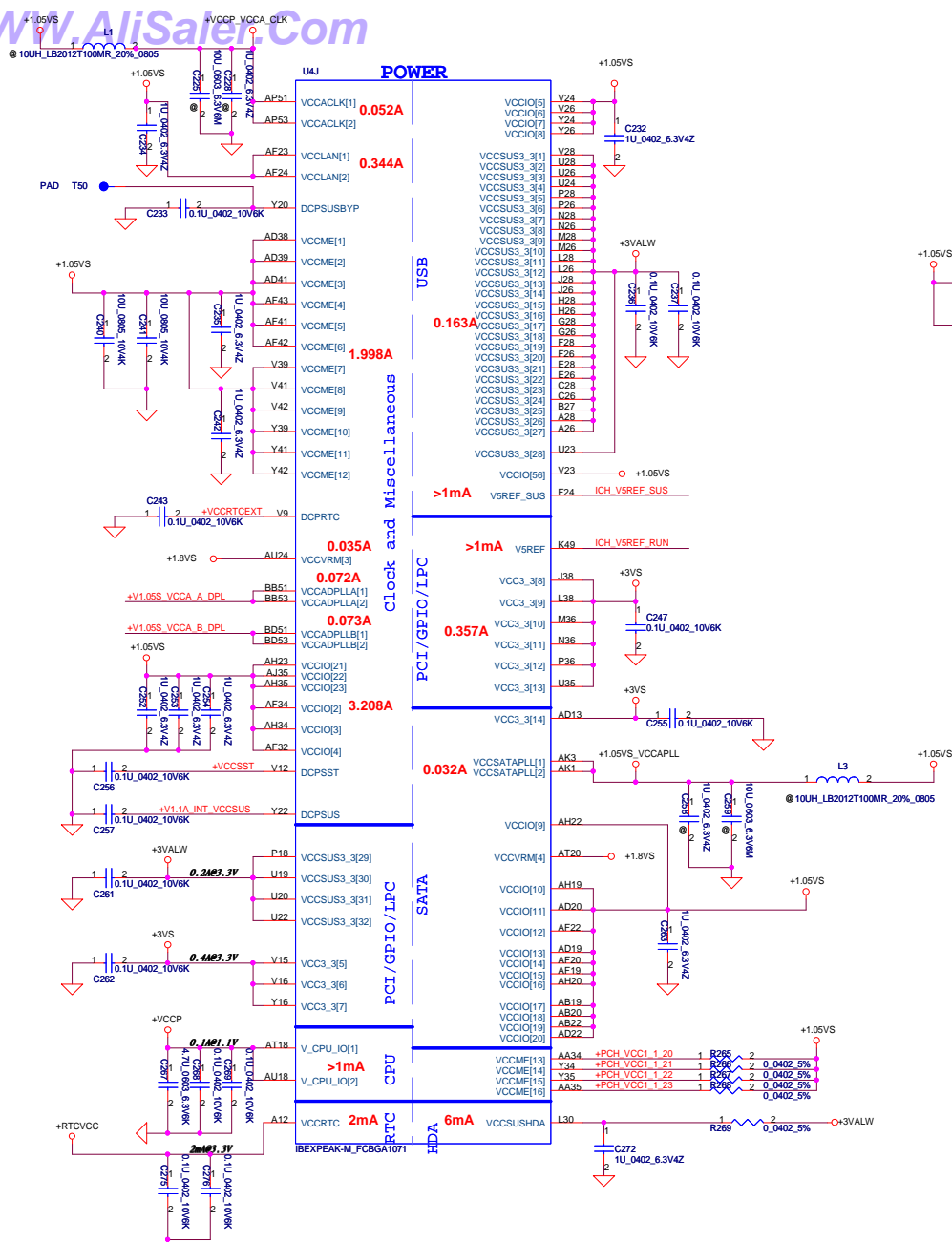


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				Custom	LA-4891
				Date:	Monday, October 27, 2008
				Sheet	14 of 50
				Rev	0.1

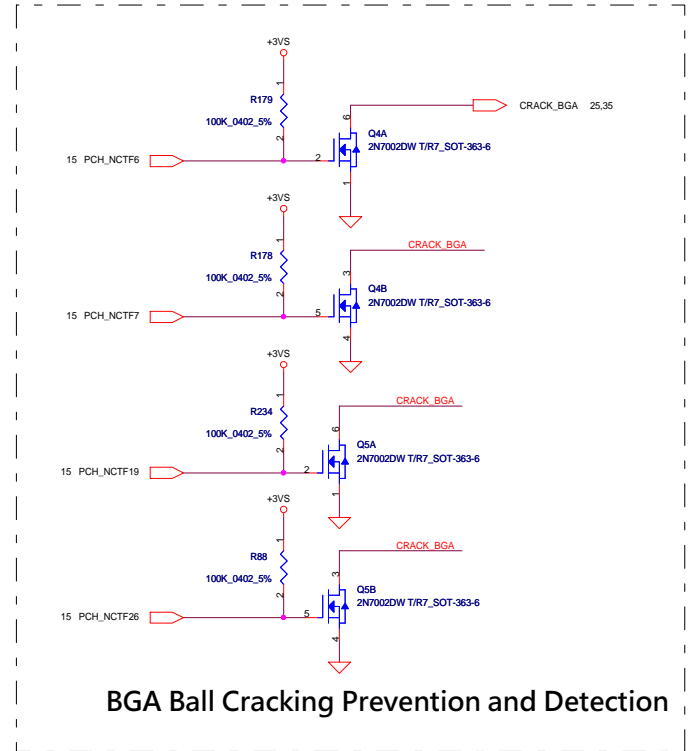
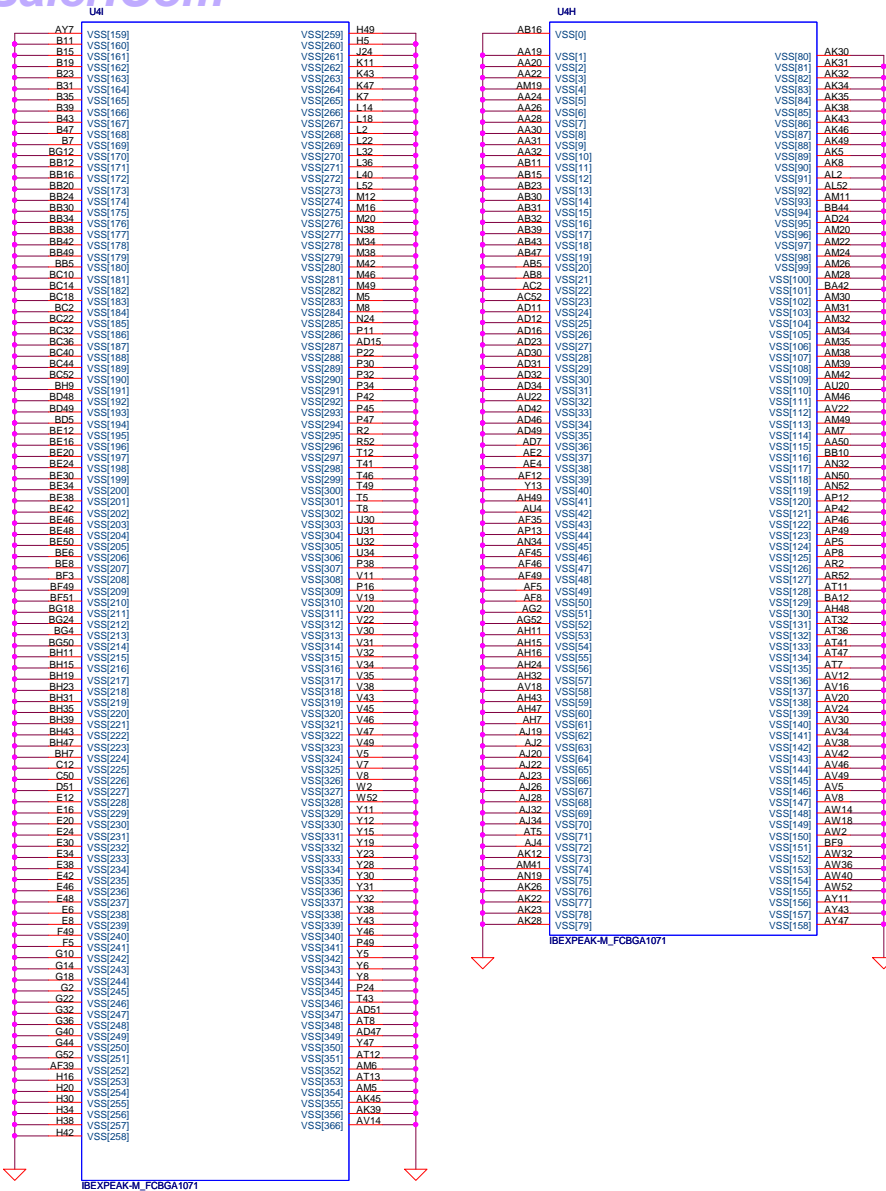






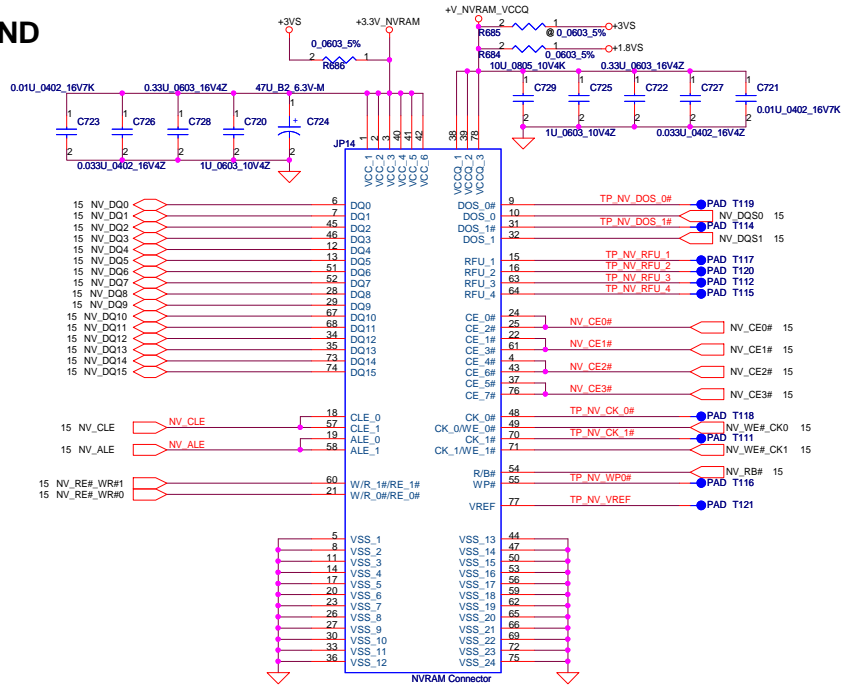


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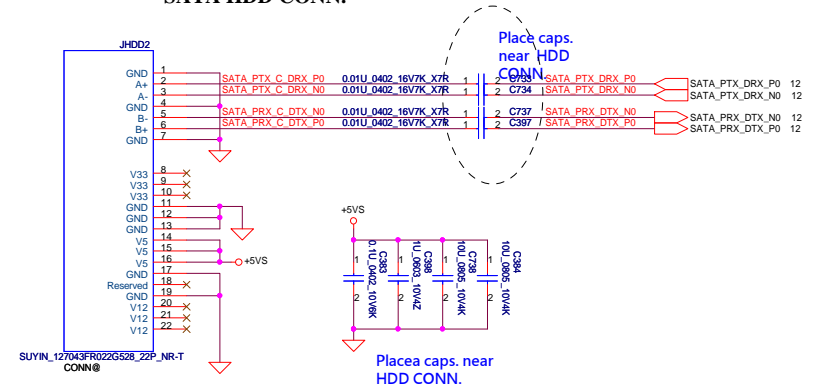


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				Date: Monday, October 27, 2008	Sheet 17 of 50

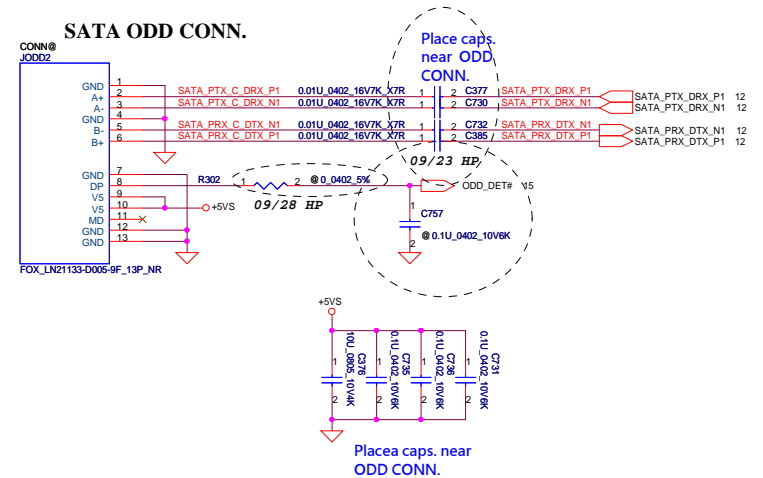
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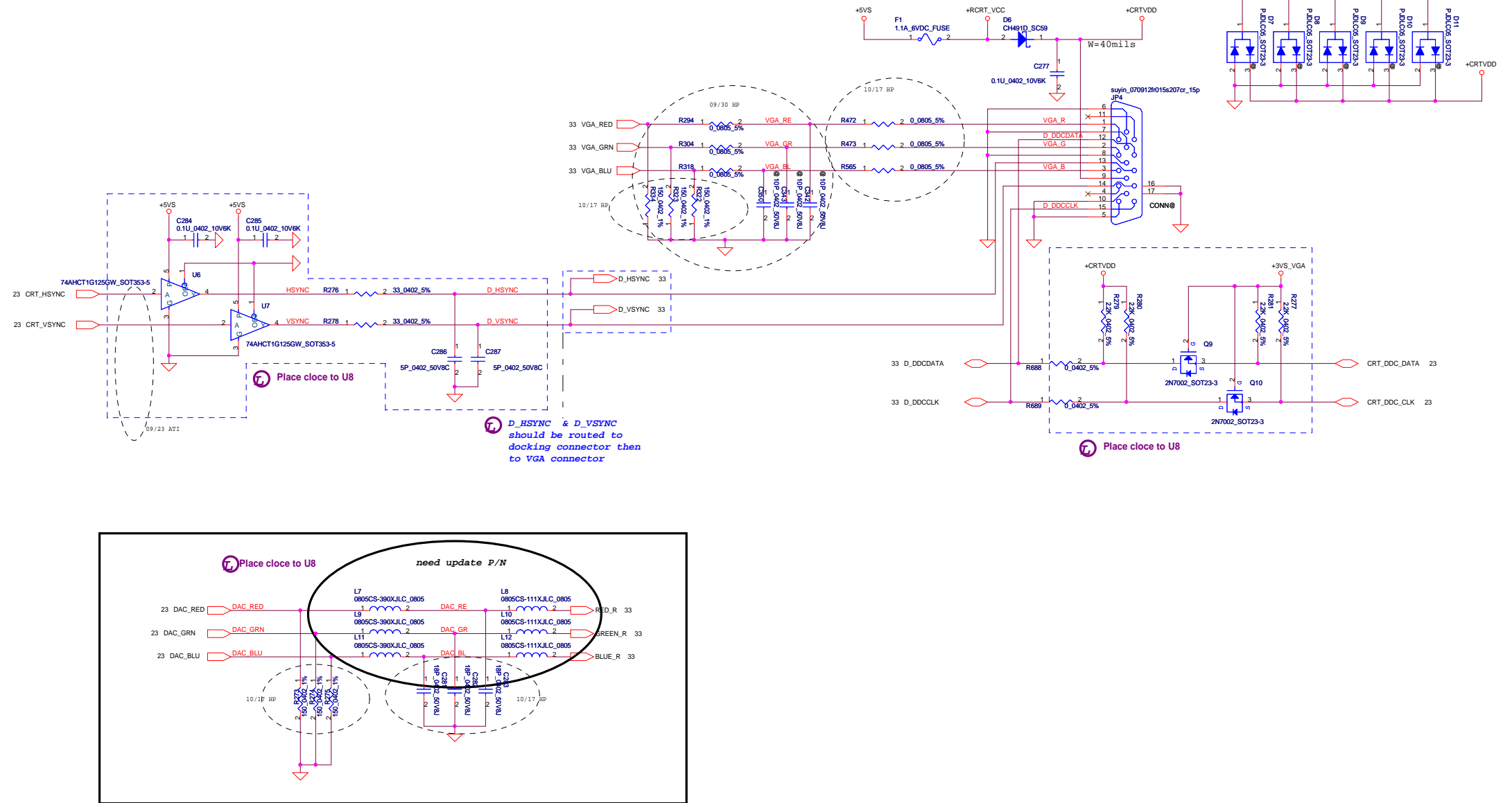
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## SATA ODD CONN.

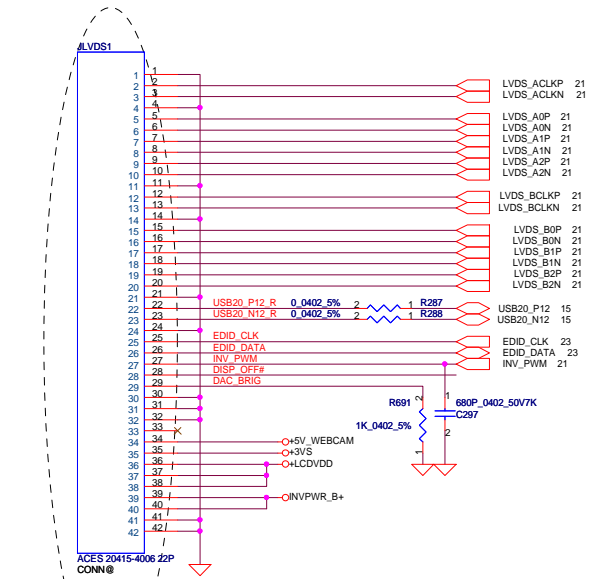


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Size	Custom	Document Number	LA-4891	Rvw
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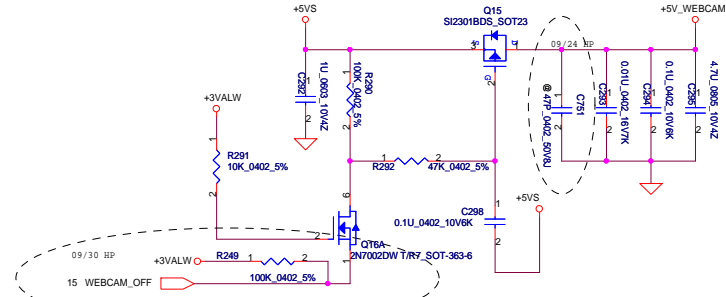
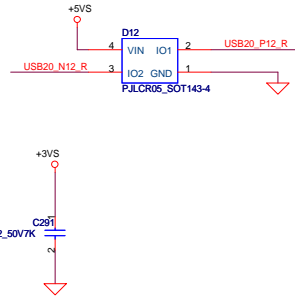
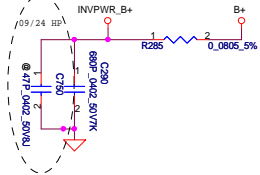
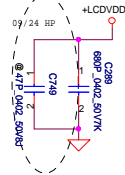


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Date: Monday, October 27, 2008		Sheet 19 of 50		Title	
				CRT Connector	

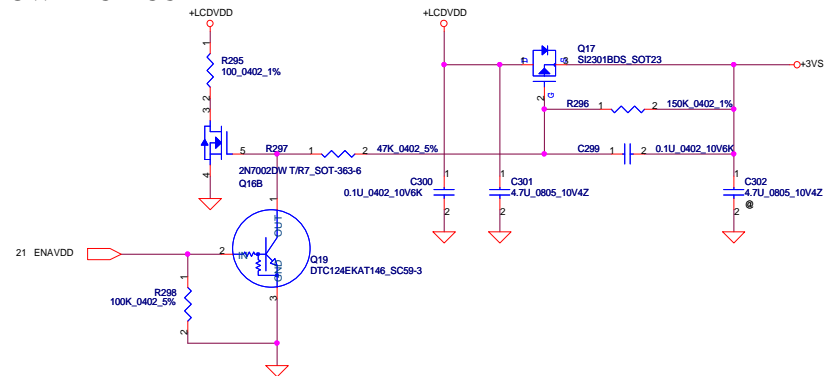
# LCD/PANEL BD. CONN.



10/01 Change the footprint

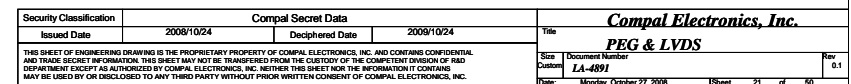


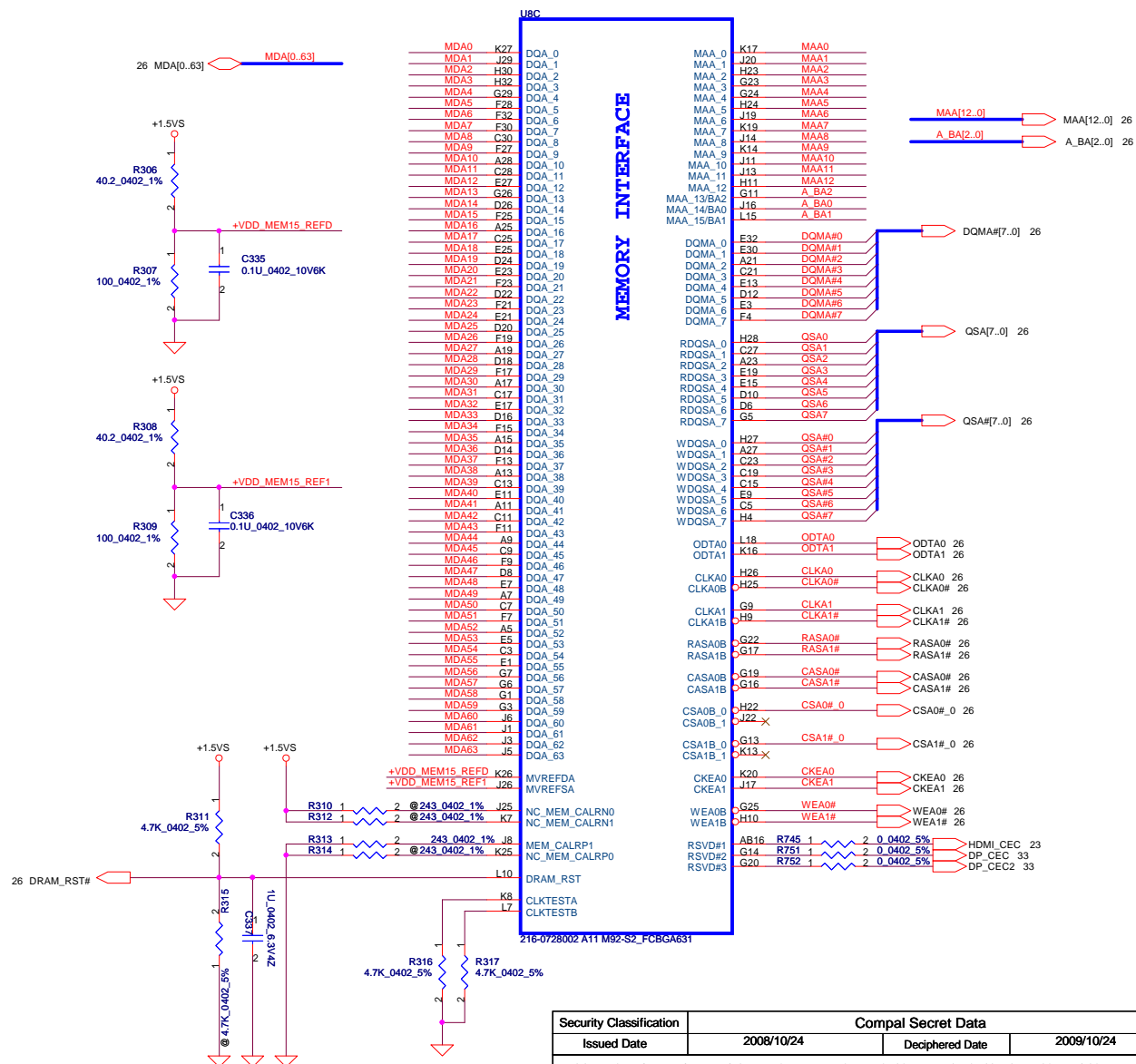
## LCD POWER CIRCUIT



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Date: Monday, October 27, 2008				Sheet 20 of 50

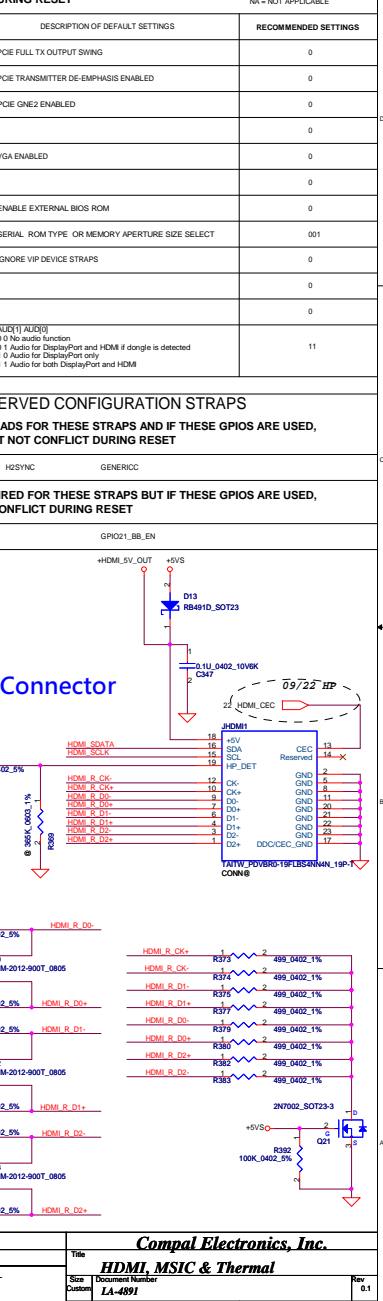
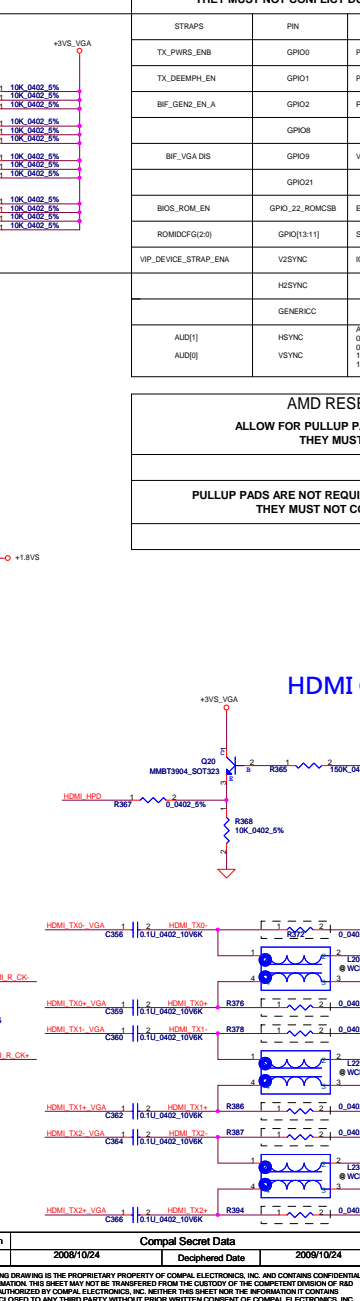
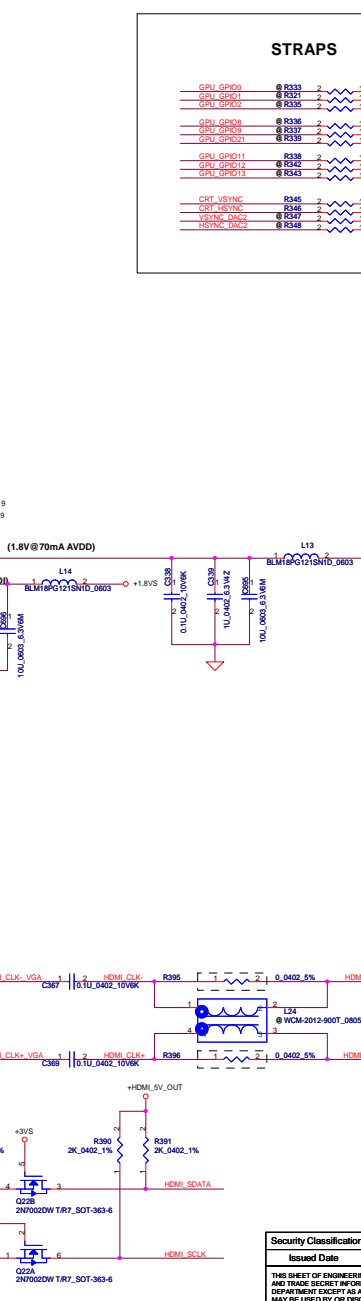
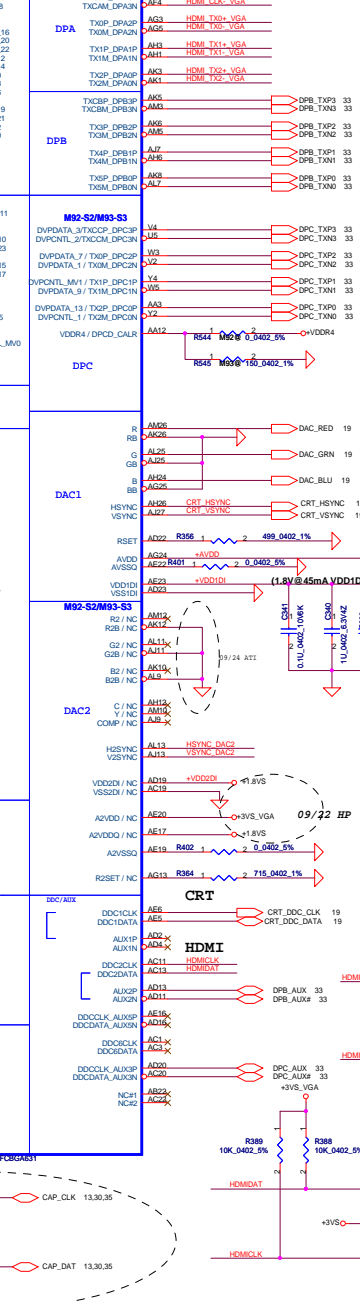
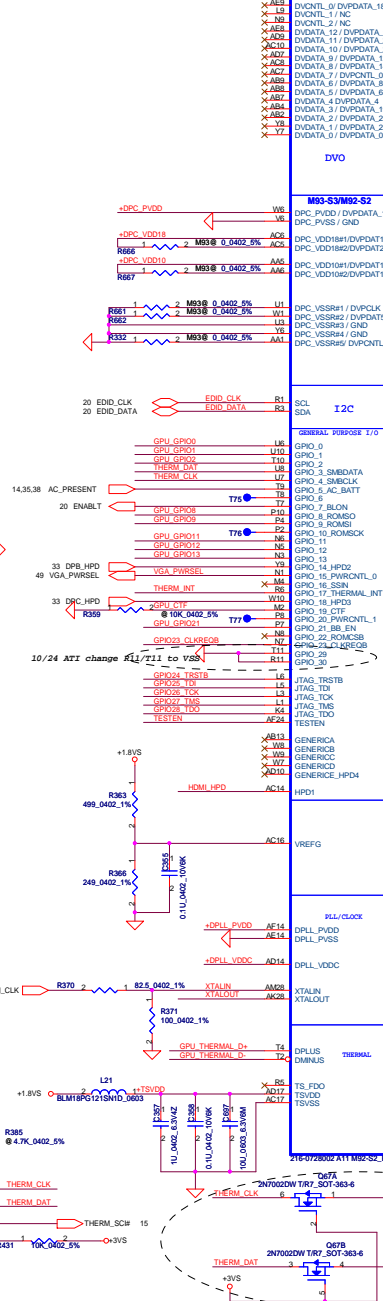
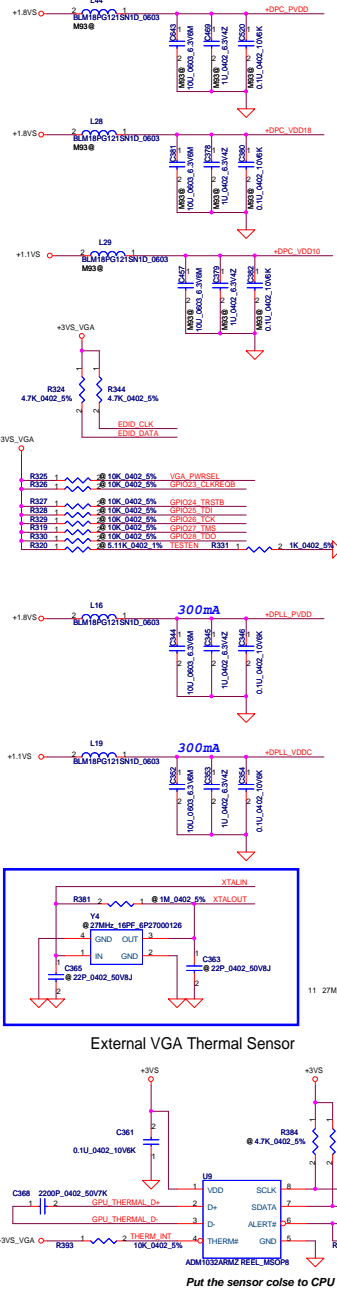
## PCI EXPRESS INTERFACE





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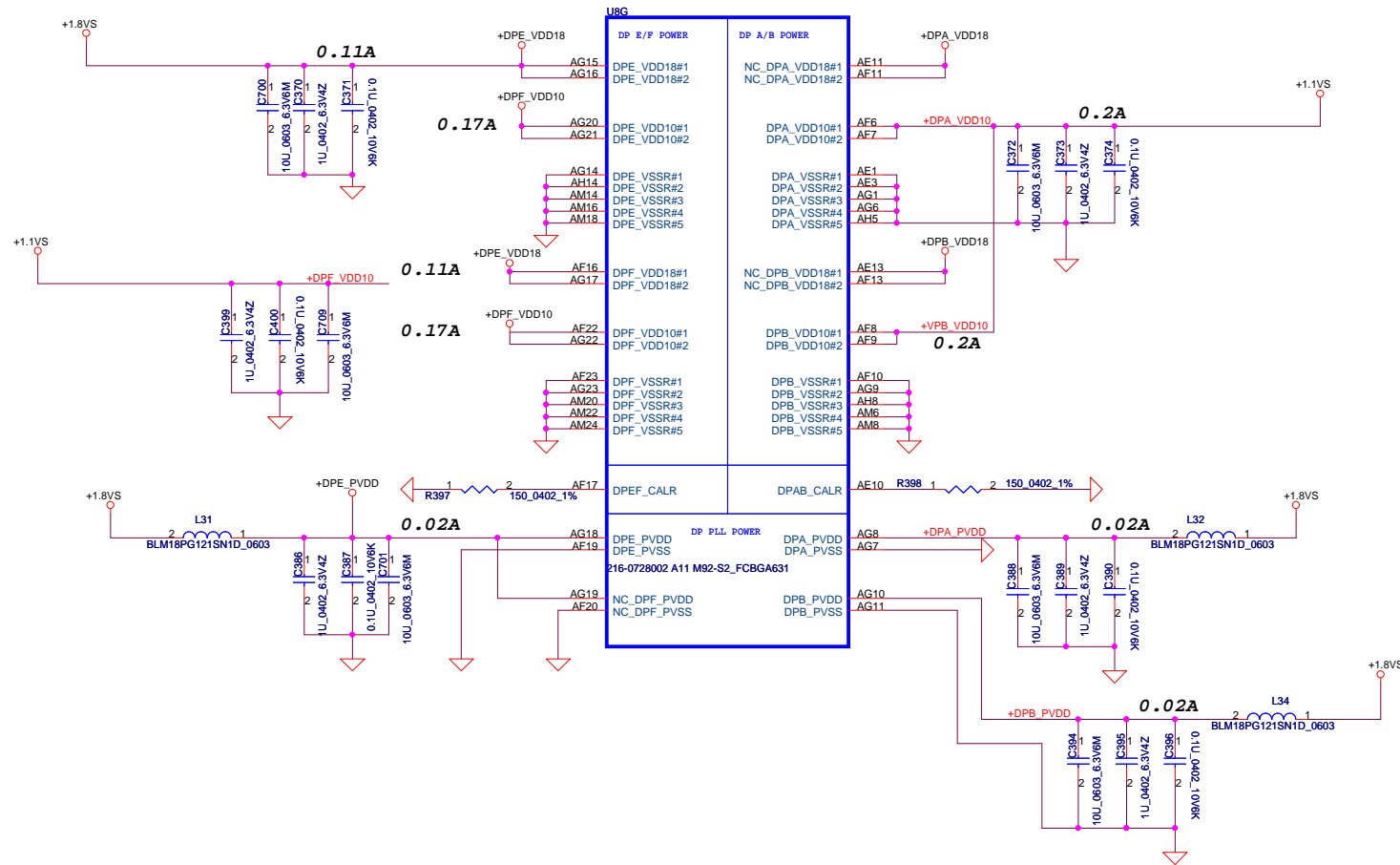


CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0 = DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PRRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	0
	GPIO3		0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMDCFG2(2:0)	GPIO(1:3:1)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001
VP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VP DEVICE STRAPS	0
	H2SYNC		0
	GENERICC		0
AUD[1]	HSYNC	AUD[0] AUDIO 0 0 No audio function 1 0 Audio for DisplayPort and HDMI if dongle is detected	11
AUD[0]	VSYNC	1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	

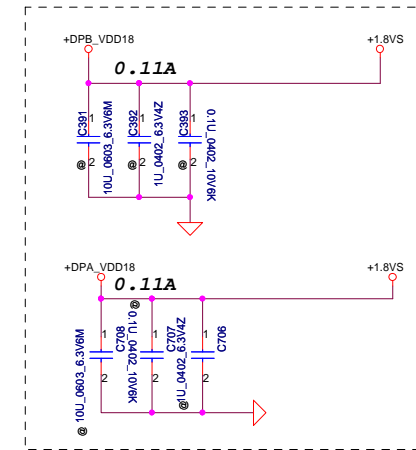
<p align="center"><b>AMD RESERVED CONFIGURATION STRAPS</b></p> <p align="center"><b>ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET</b></p>	
HS07YC	GENERICC
<p align="center"><b>PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET</b></p>	
GPIO21_BB_EN	

[illegible][illegible]

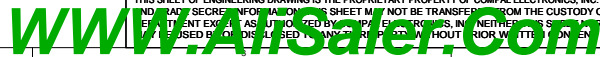
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			Sheet	23	of 50

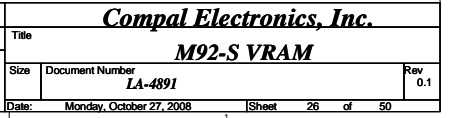


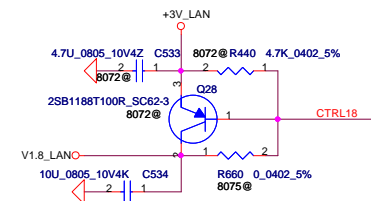
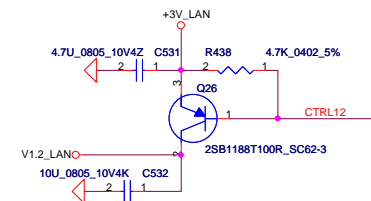
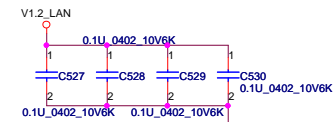
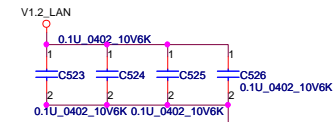
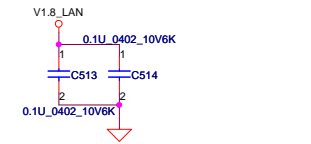
For Future S3 GPUs



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				Sheet	24 of 50
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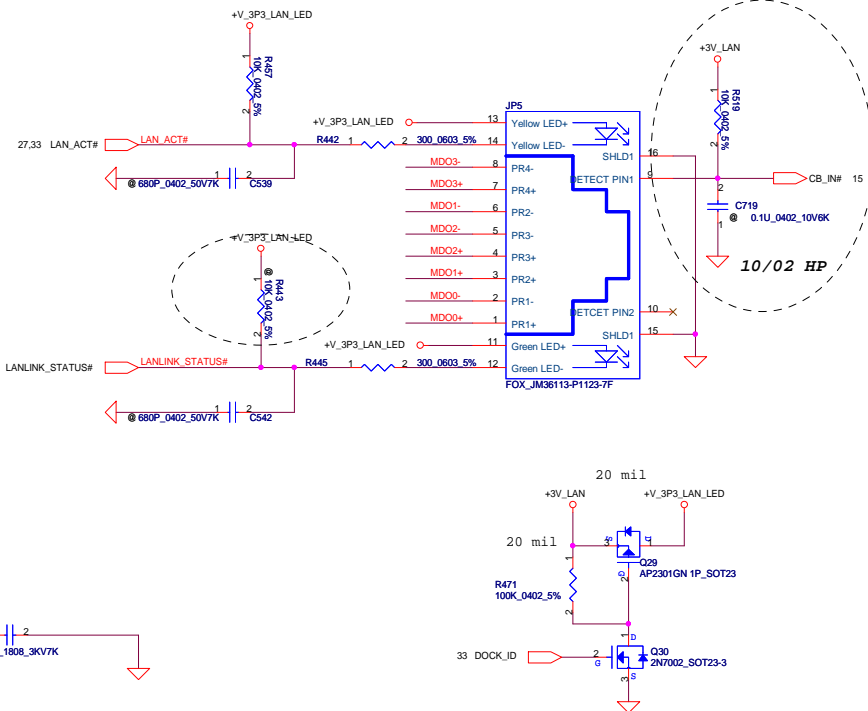


Schematic diagram of the A025F1024AN-10SU-2.7 SOIC 8P chip. The chip is a black circle with pins 1 through 8. Pin 1 is connected to C694 (01U\_0402\_10V6K) and pin 2 is connected to 8075@. Pin 3 is connected to SPI CS LAN. Pin 4 is connected to SPI DI LAN. Pin 5 is connected to SPI DO LAN. Pin 6 is connected to SPI CLK LAN. Pin 7 is connected to VCC. Pin 8 is connected to HOLD#. The chip is labeled U36 and A025F1024AN-10SU-2.7 SOIC 8P 8075@.

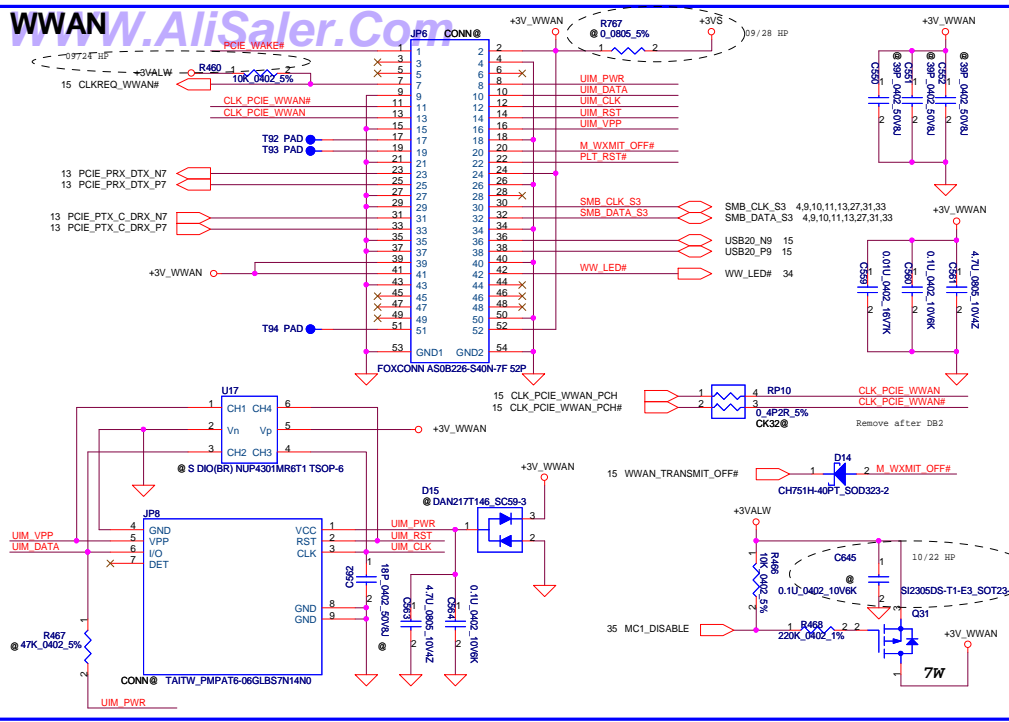
ROM size will update  
after check with vendor

	<b>Compal Electronics, Inc.</b>
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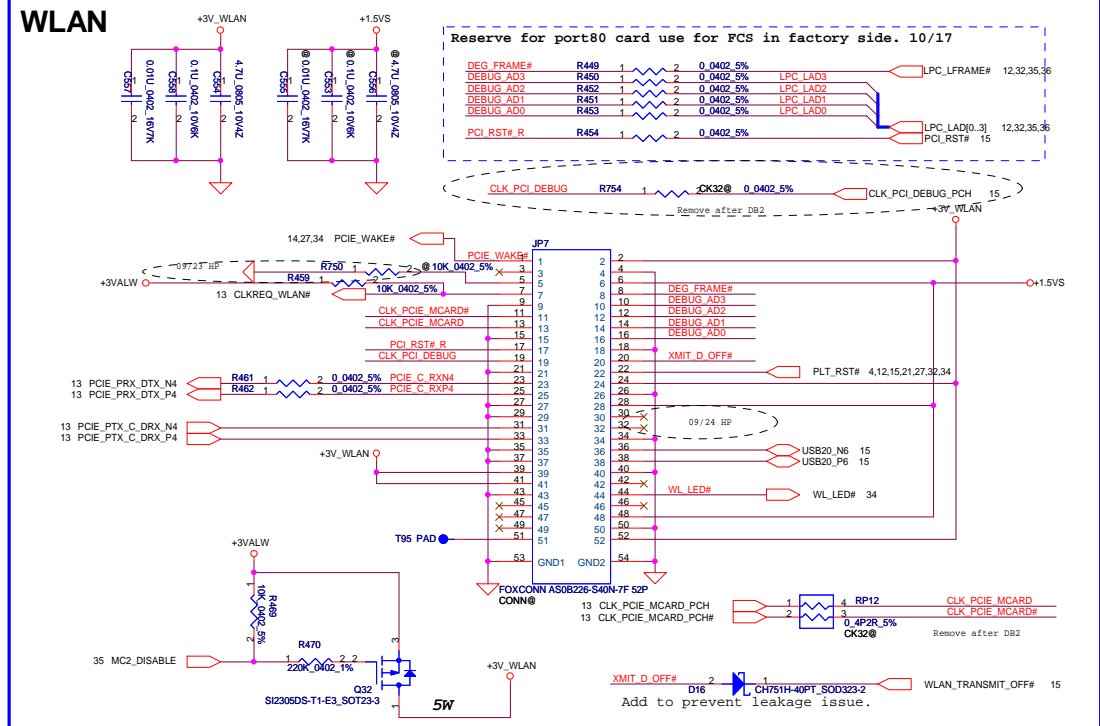
10/02 HP



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				Size		Document Number <b>LA-4891</b>
				Date:	Thursday, October 30, 2008	Sheet

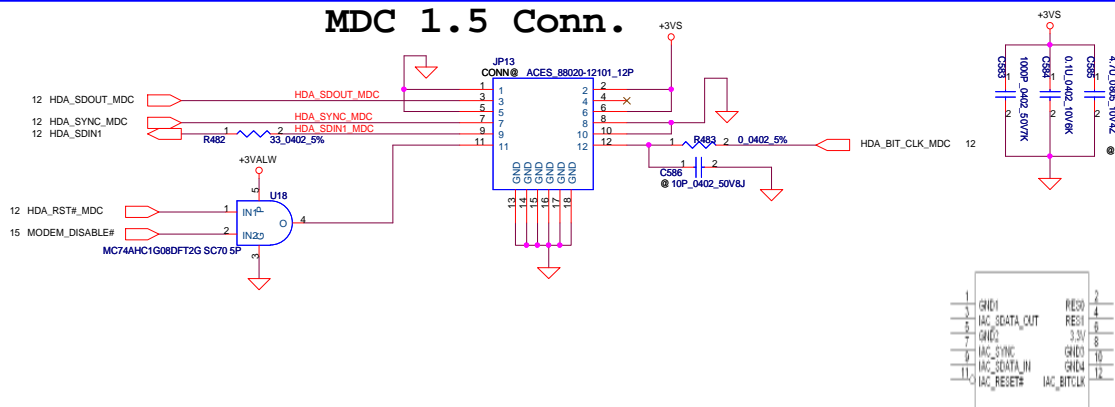
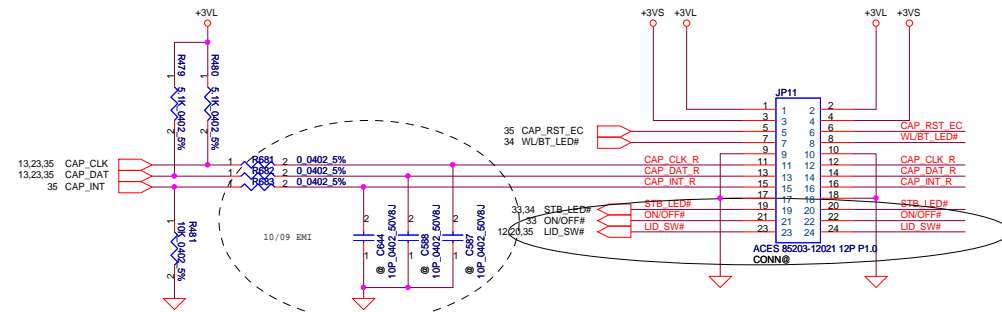


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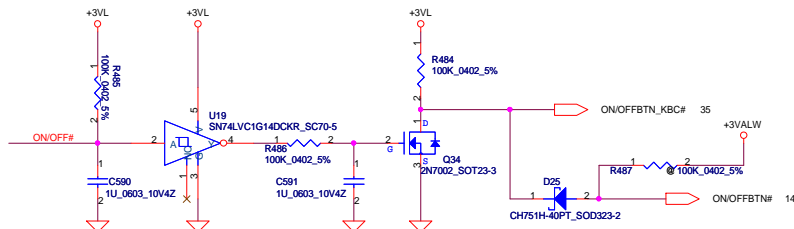


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						Size		Document Number		Rev	
						Date:		Wednesday, October 29, 2008		Sheet 29 of 50	
				LA-4891		0.1					

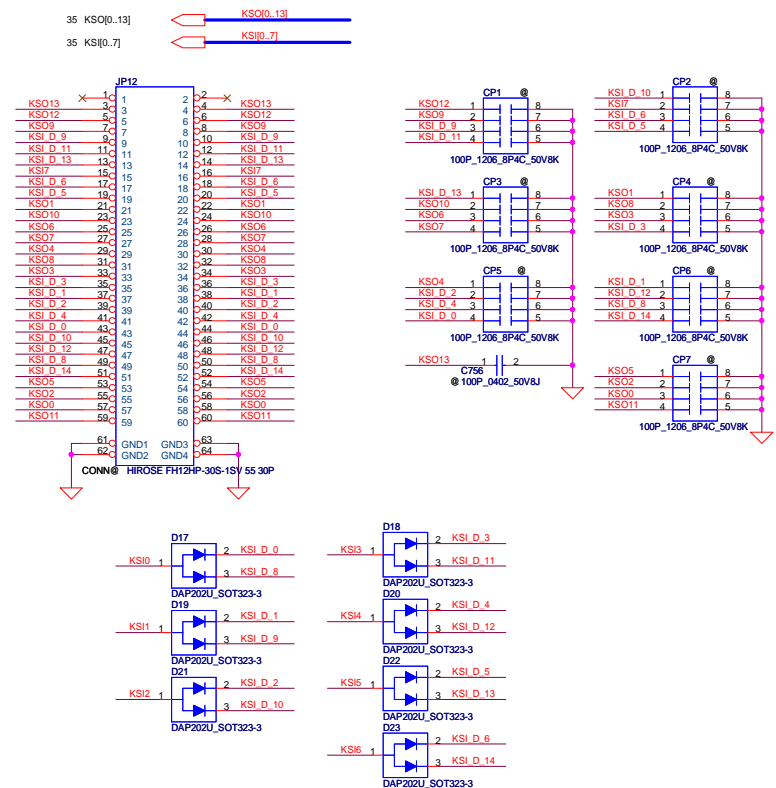




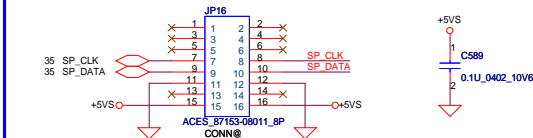
## Power button



## INT\_KBD\_CONN.



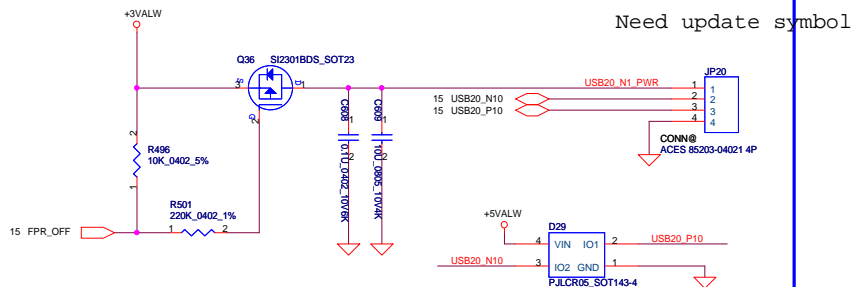
## TrackPoint CONN.



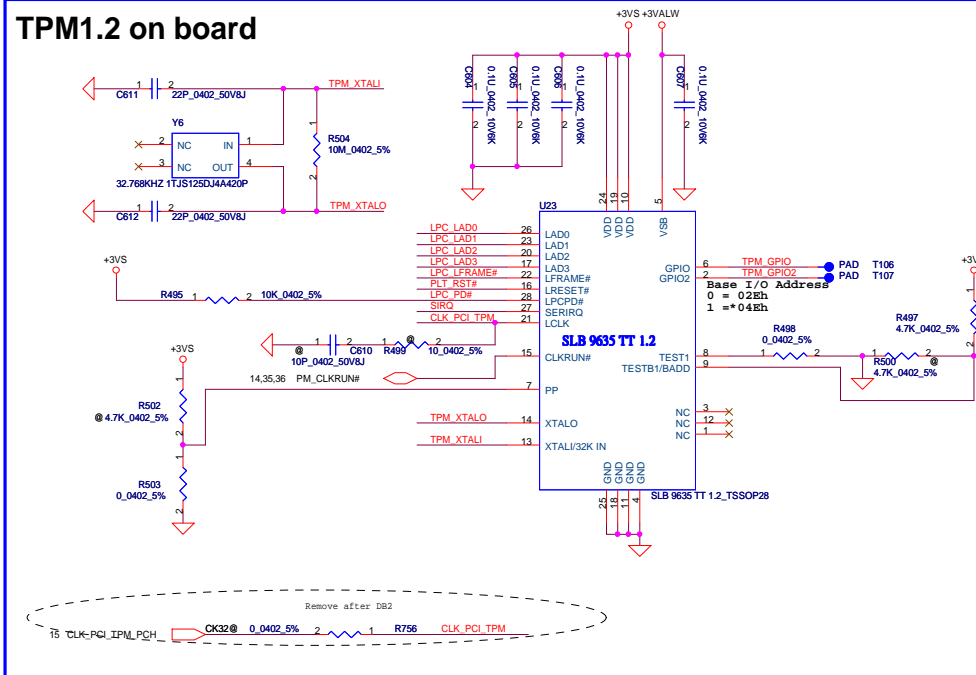
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Issued Date	2008/10/24	Deciphered Date	2009/10/24	Title		
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				Size	Document Number	Rev
				<b>LA-491</b>		<b>0.1</b>
Date				Monday	October 27, 2008	Sheet 30 of 50



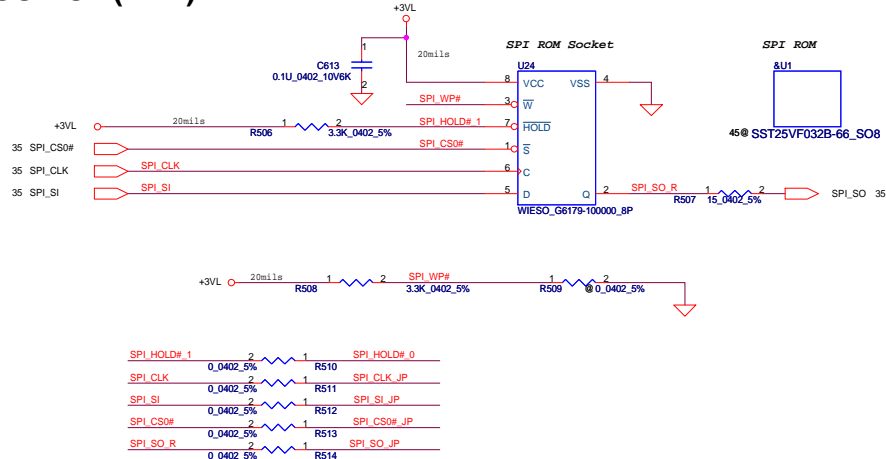
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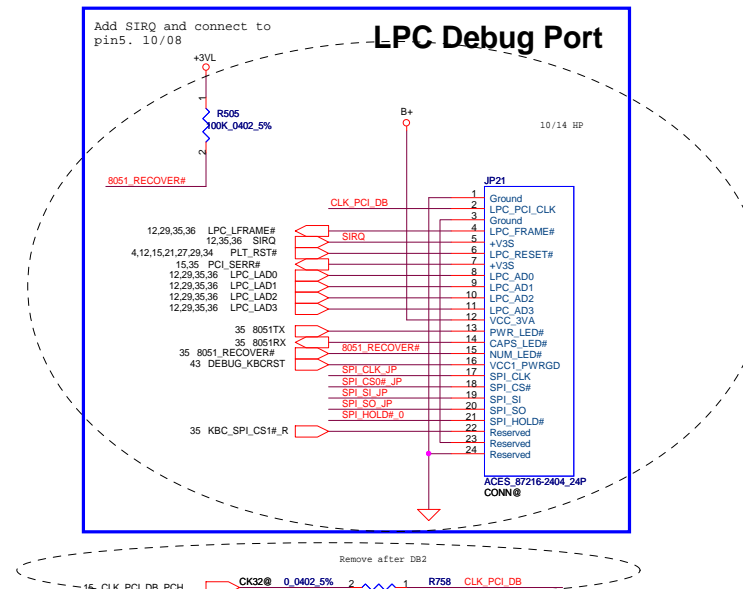
## TPM1.2 on board



**BIOS ROM(4MB)**

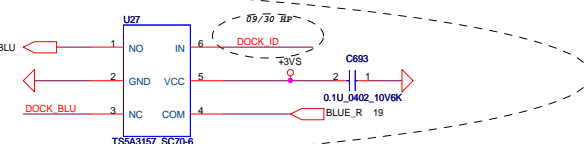
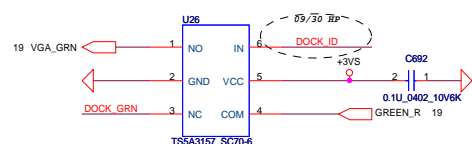
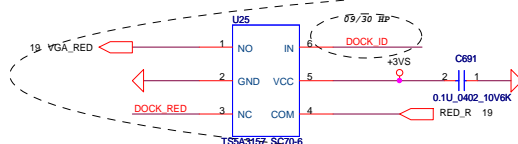
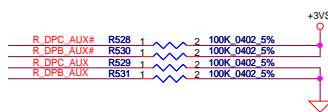
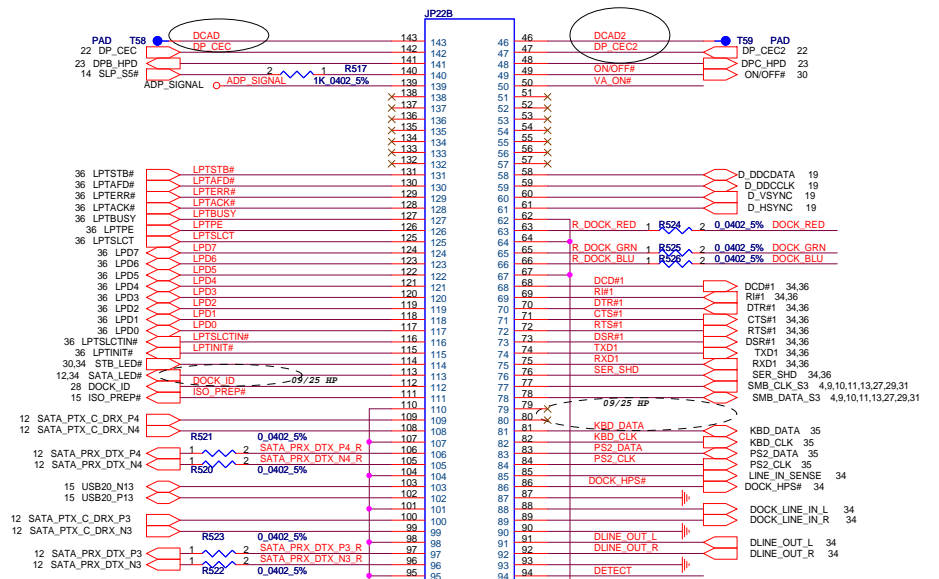
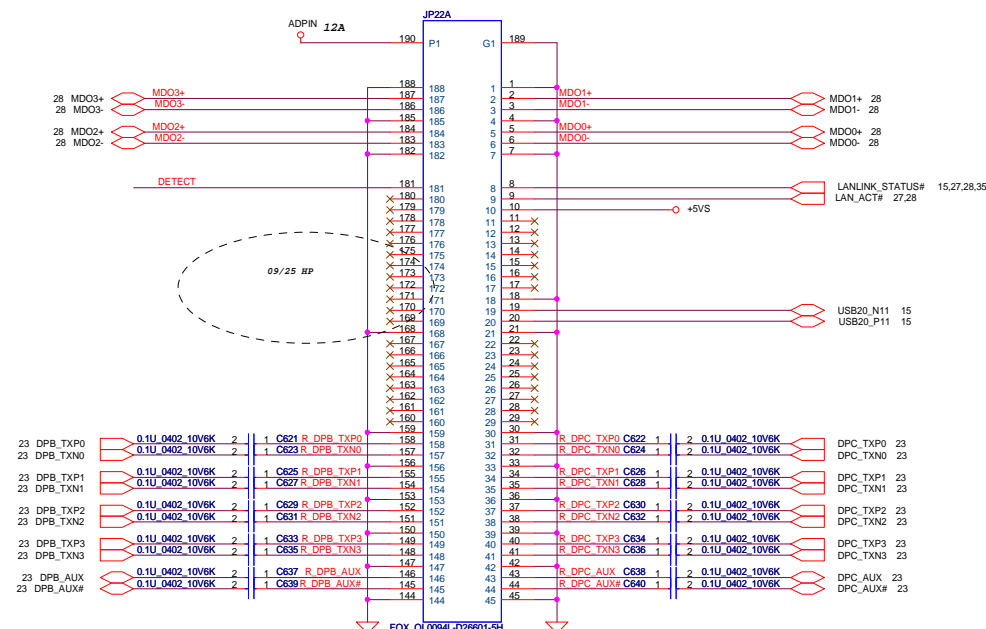
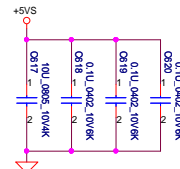
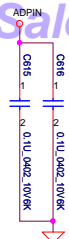


## - LPC Debug Port



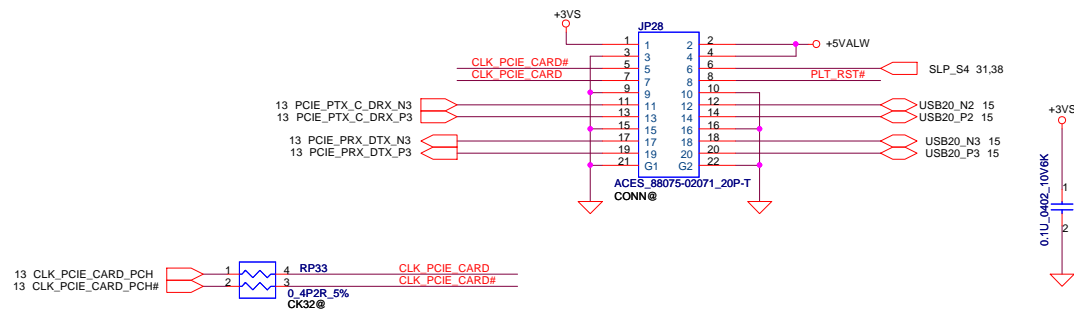
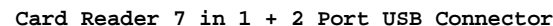
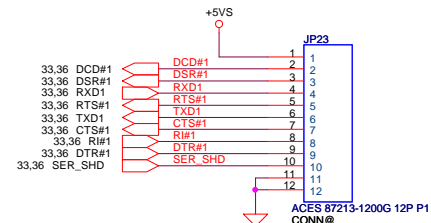
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- (2) PS/2 Interfaces
- (2) USB 2.0 channels
- (2) SATA Channels
- (2) Display Port Channels
- (1) Serial Port
- (1) Parallel Port
- (1) Line In
- (1) Line Out
- (1) RJ45 (10/100/1000)
- (1) VGA
- (1) 2 LAN indicator LED's
- (1) Power Button
- (1) I2C interface

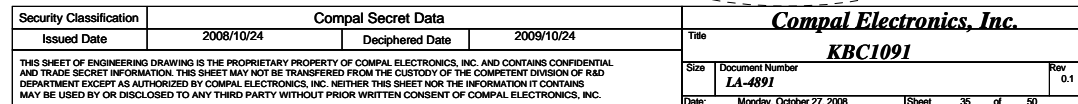


IN	NC<-->COM	NO<-->COM
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H	OFF	ON

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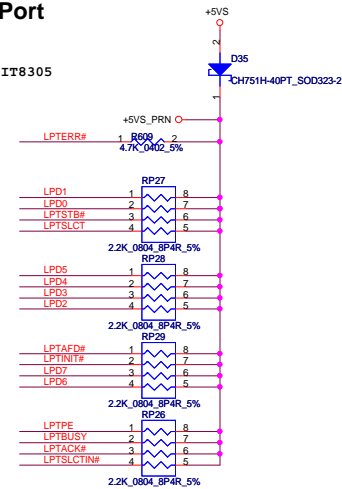


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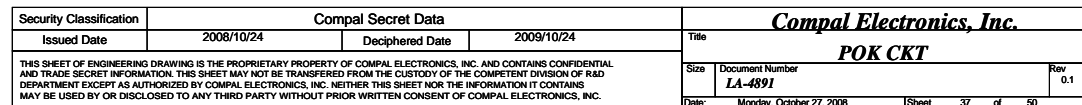
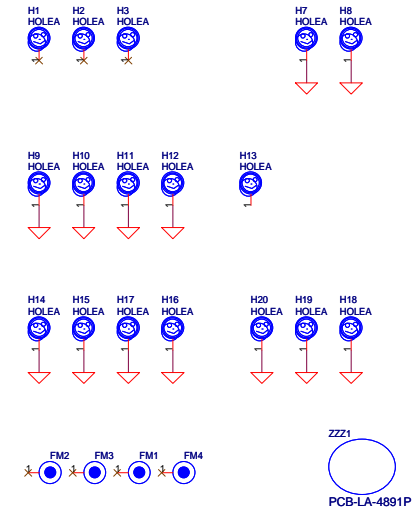


+5VS  
2  
D35  
CH751H-40PT\_SOD323-2

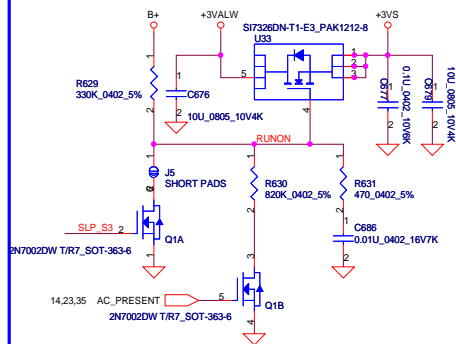


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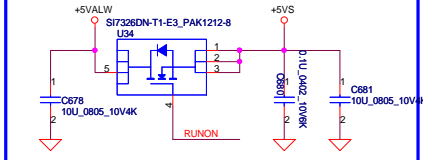




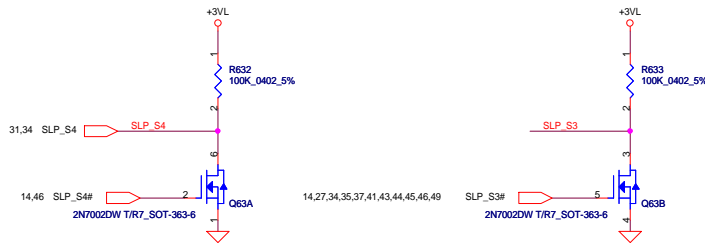
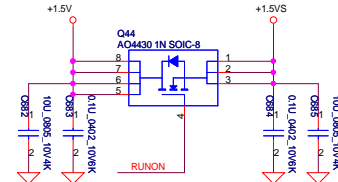
### +3VALW to +3VS Transfer



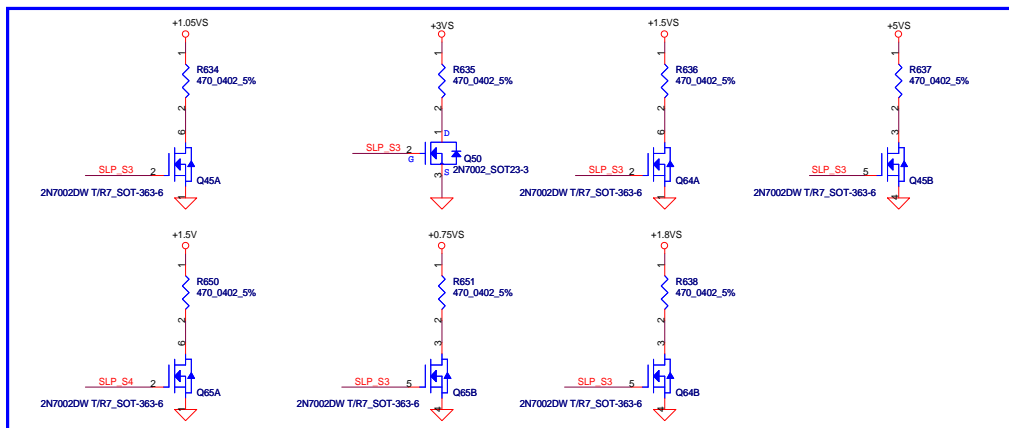
### +5VALW to +5VS Transfer



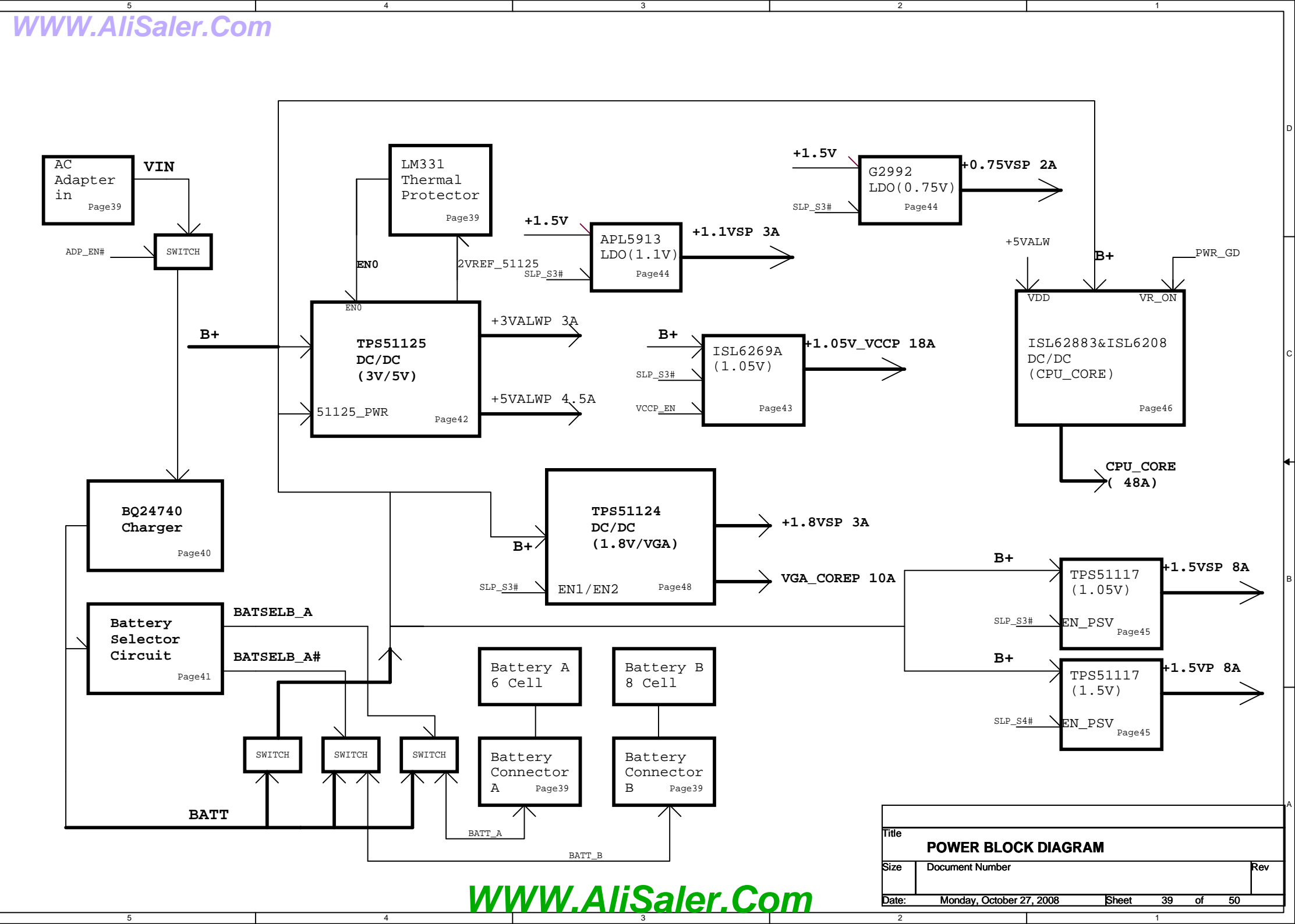
### +1.5V to +1.5VS Transfer



### Discharge circuit-1



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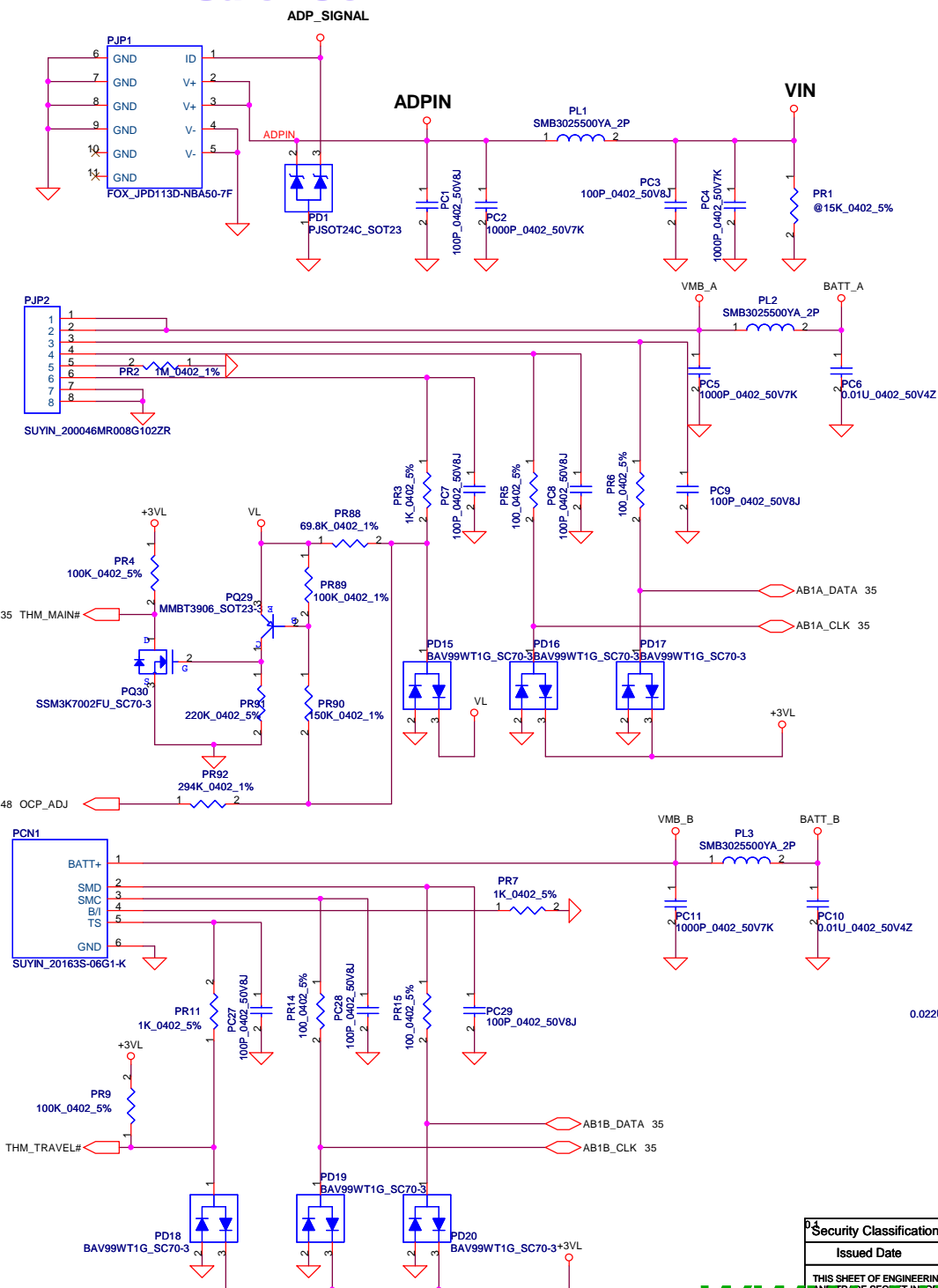
The diagram illustrates a power management system with the following components and connections:

- AC Adapter in** (Page 39) provides **VIN** to a **SWITCH**.
- BQ24740 Charger** (Page 40) is connected to the **BATT** line.
- Battery Selector Circuit** (Page 41) manages **Battery A** (6 Cell) and **Battery B** (8 Cell) via **Battery Connector A** and **Battery Connector B** (Page 39).
- TPS51125 DC/DC (3V/5V)** (Page 42) receives **B+** and **51125\_PWR** signals. It outputs **+3VALWP 3A** and **+5VALWP 4.5A**.
- LM331 Thermal Protector** (Page 39) is connected to the **TPS51125** and provides **2VREF\_51125** to the **APL5913 LDO(1.1V)** (Page 44).
- APL5913 LDO(1.1V)** (Page 44) receives **+1.5V** and **SLP\_S3#** signals, outputting **+1.1VSP 3A**.
- ISL6269A (1.05V)** (Page 43) receives **B+** and **SLP\_S3#** signals, outputting **+1.05V\_VCCP 18A**.
- G2992 LDO(0.75V)** (Page 44) receives **+1.5V** and **SLP\_S3#** signals, outputting **+0.75VSP 2A**.
- ISL62883&ISL6208 DC/DC (CPU\_CORE)** (Page 46) receives **+5VALW** and **B+** signals, outputting **CPU\_CORE (48A)**.
- TPS51124 DC/DC (1.8V/VGA)** (Page 48) receives **B+** and **SLP\_S3#** signals, outputting **+1.8VSP 3A** and **VGA\_COREP 10A**.
- TPS51117 (1.05V)** (Page 45) receives **B+** and **SLP\_S3#** signals, outputting **+1.5VSP 8A**.
- TPS51117 (1.5V)** (Page 45) receives **B+** and **SLP\_S4#** signals, outputting **+1.5VP 8A**.

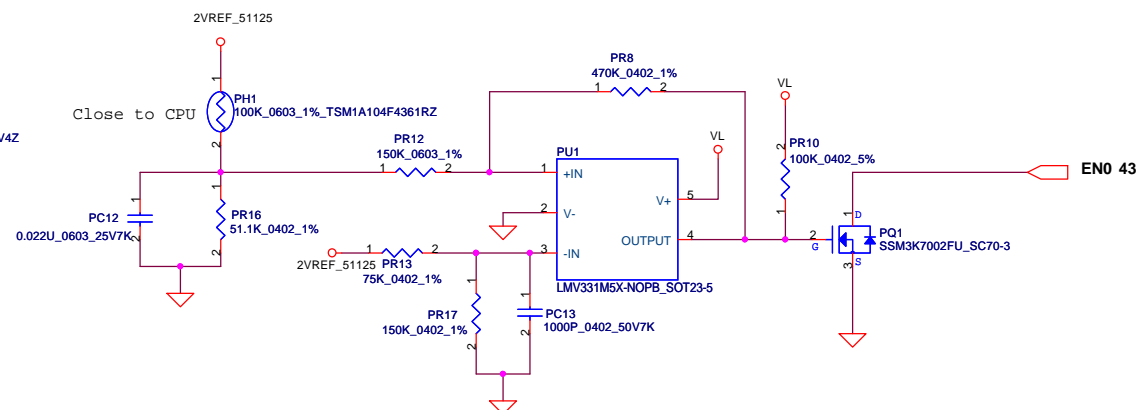
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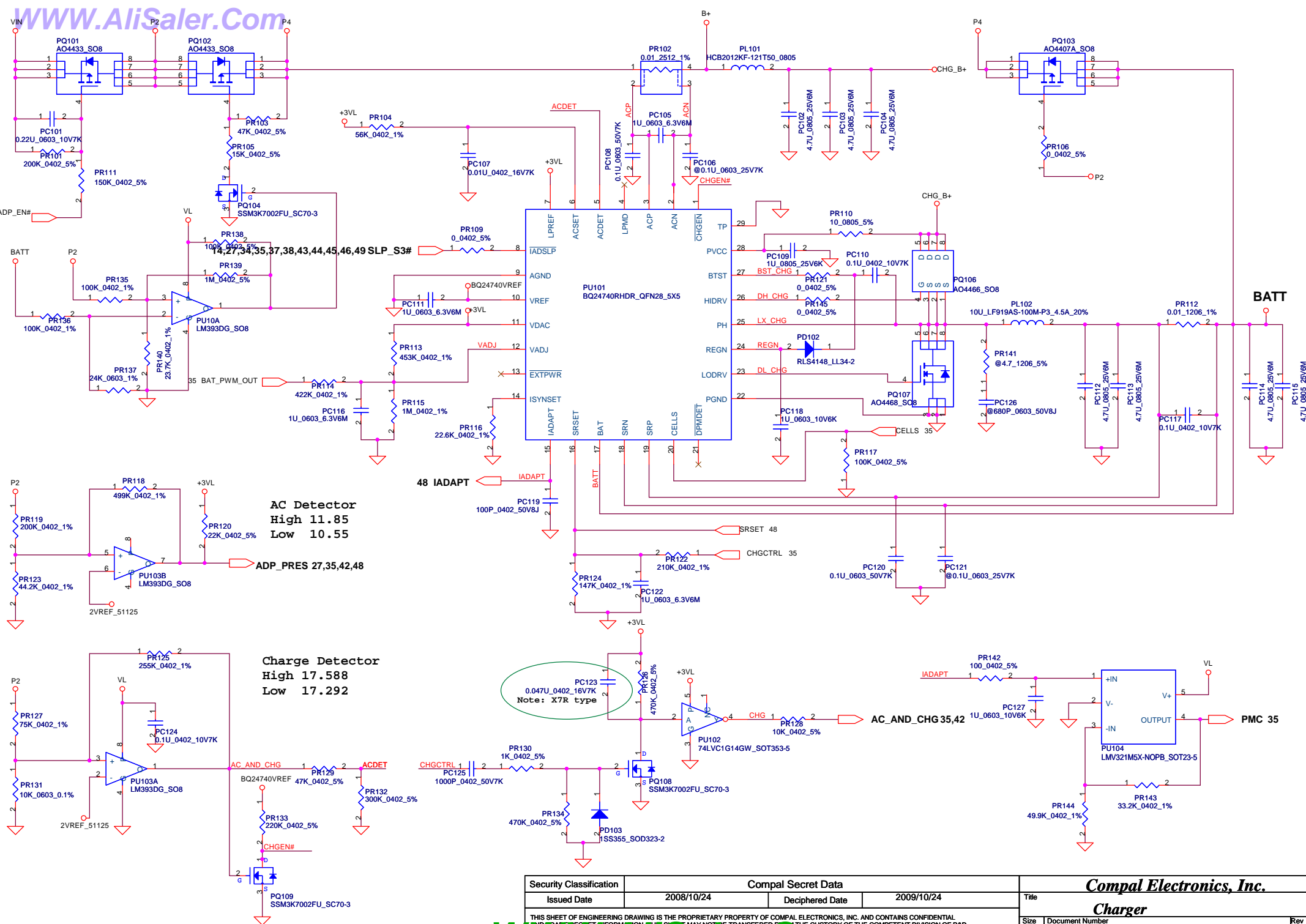
Title		
POWER BLOCK DIAGRAM		
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PH1 under CPU botten side :  
CPU thermal protection at 90 +-3 degree C  
(Need to be checked)



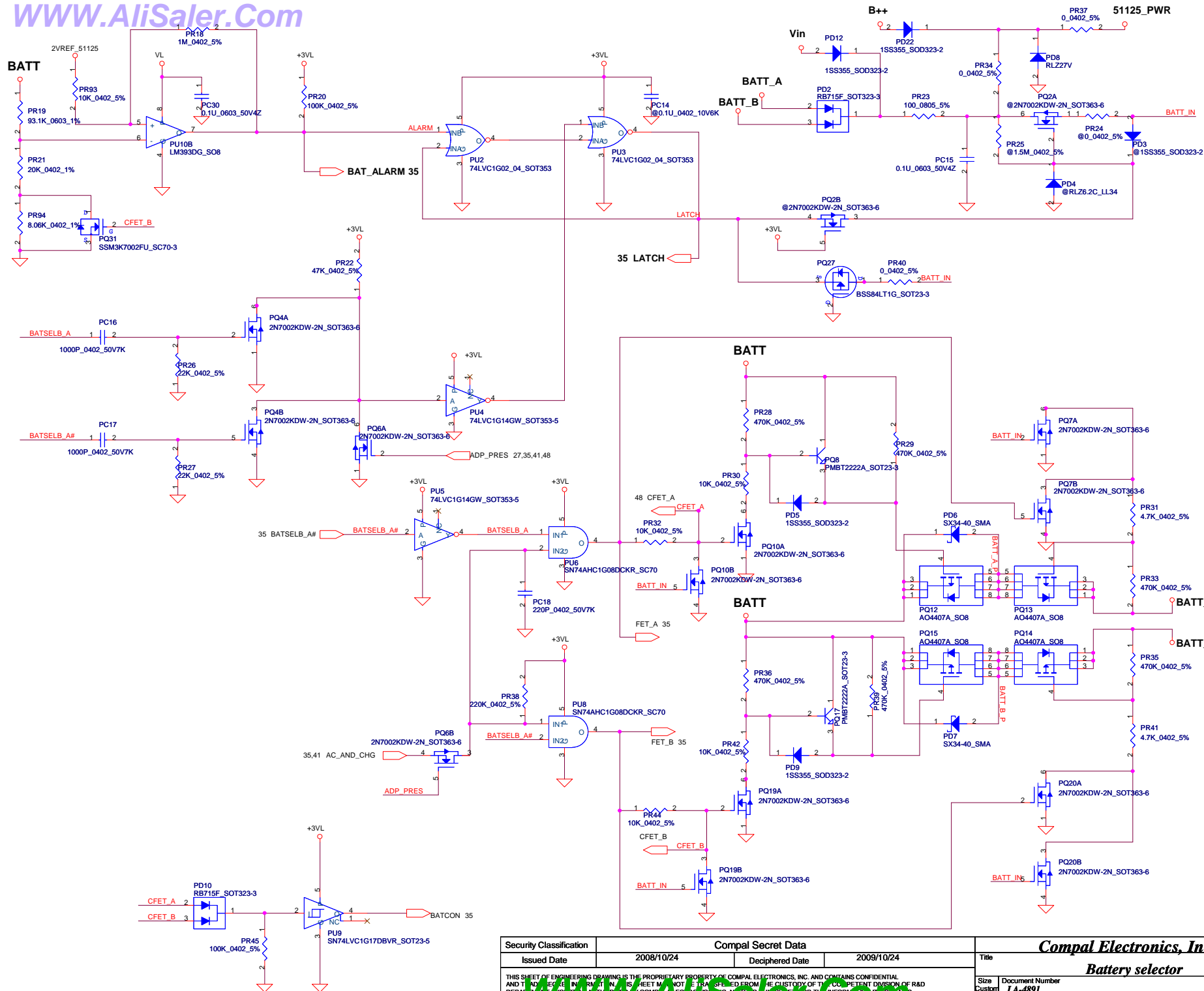
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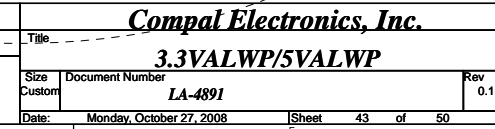
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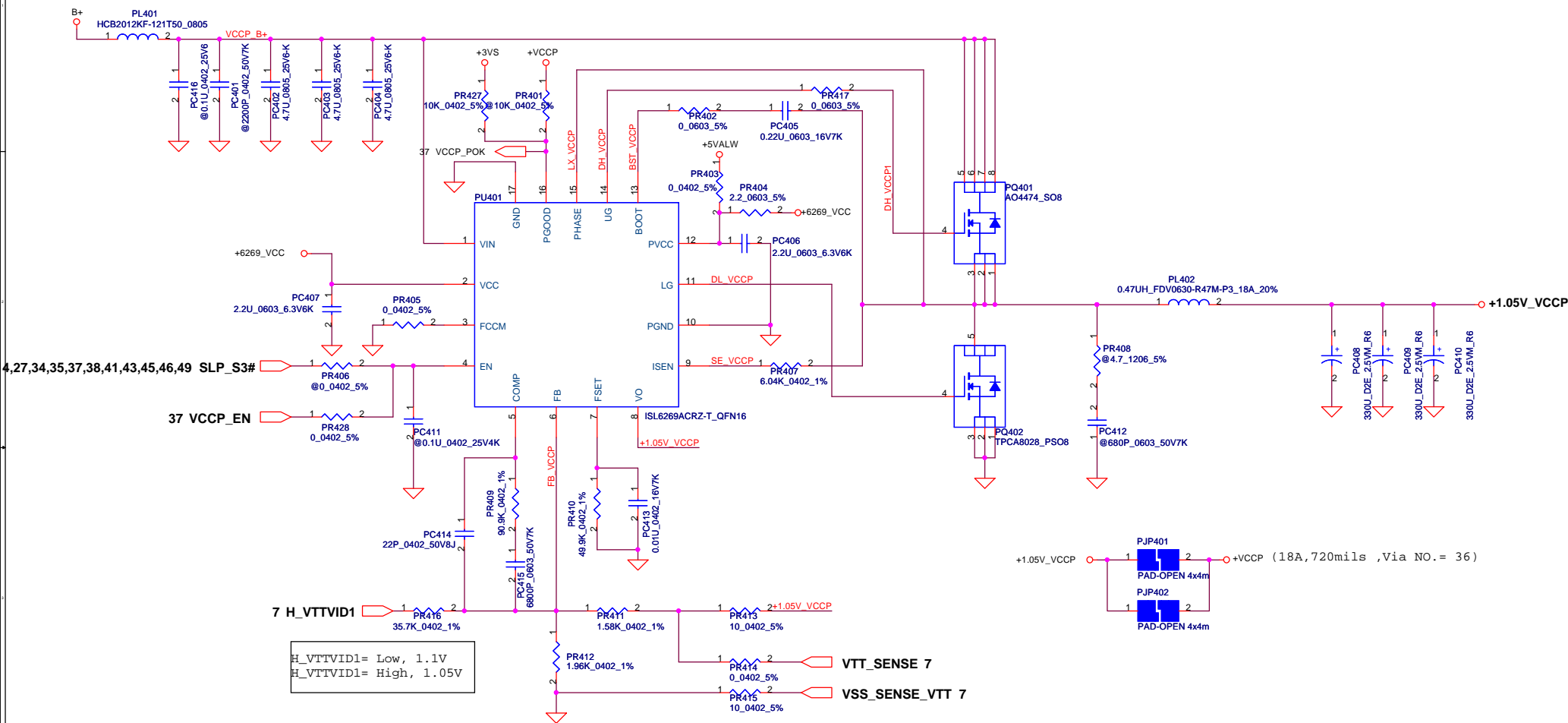
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Charger			
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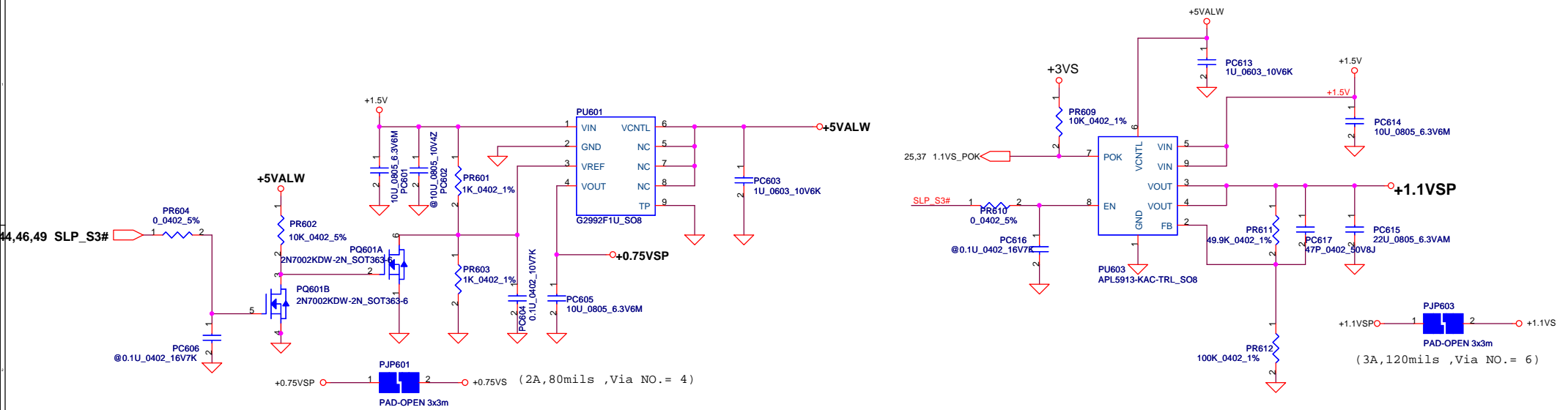
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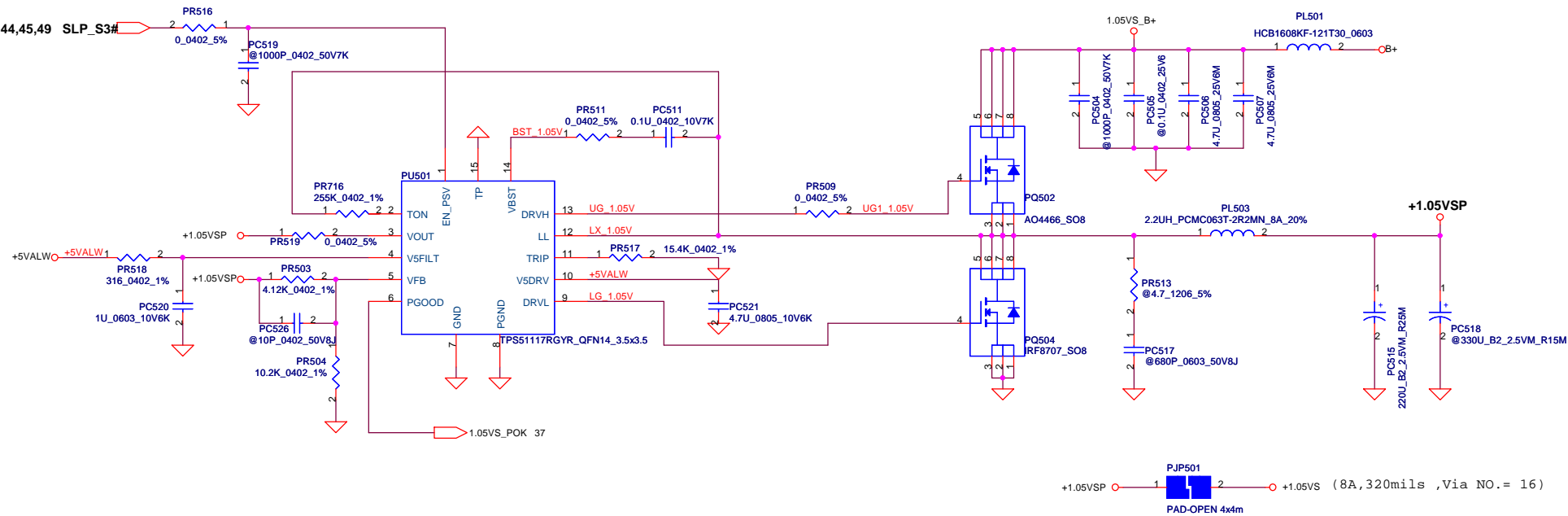


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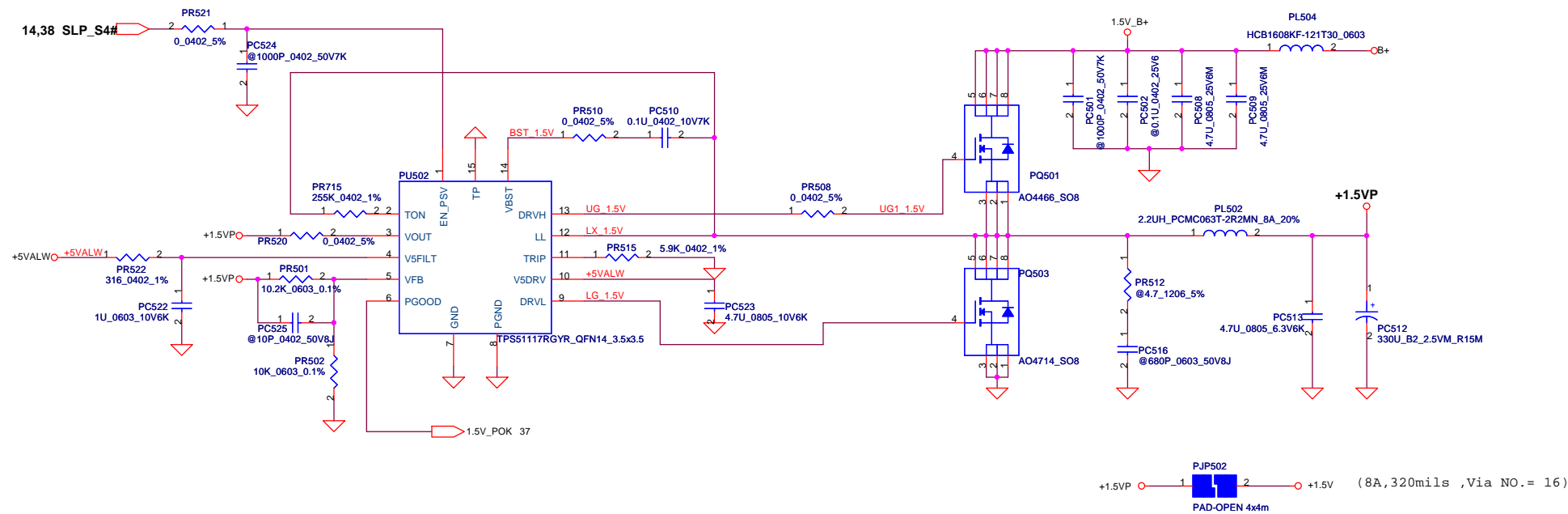


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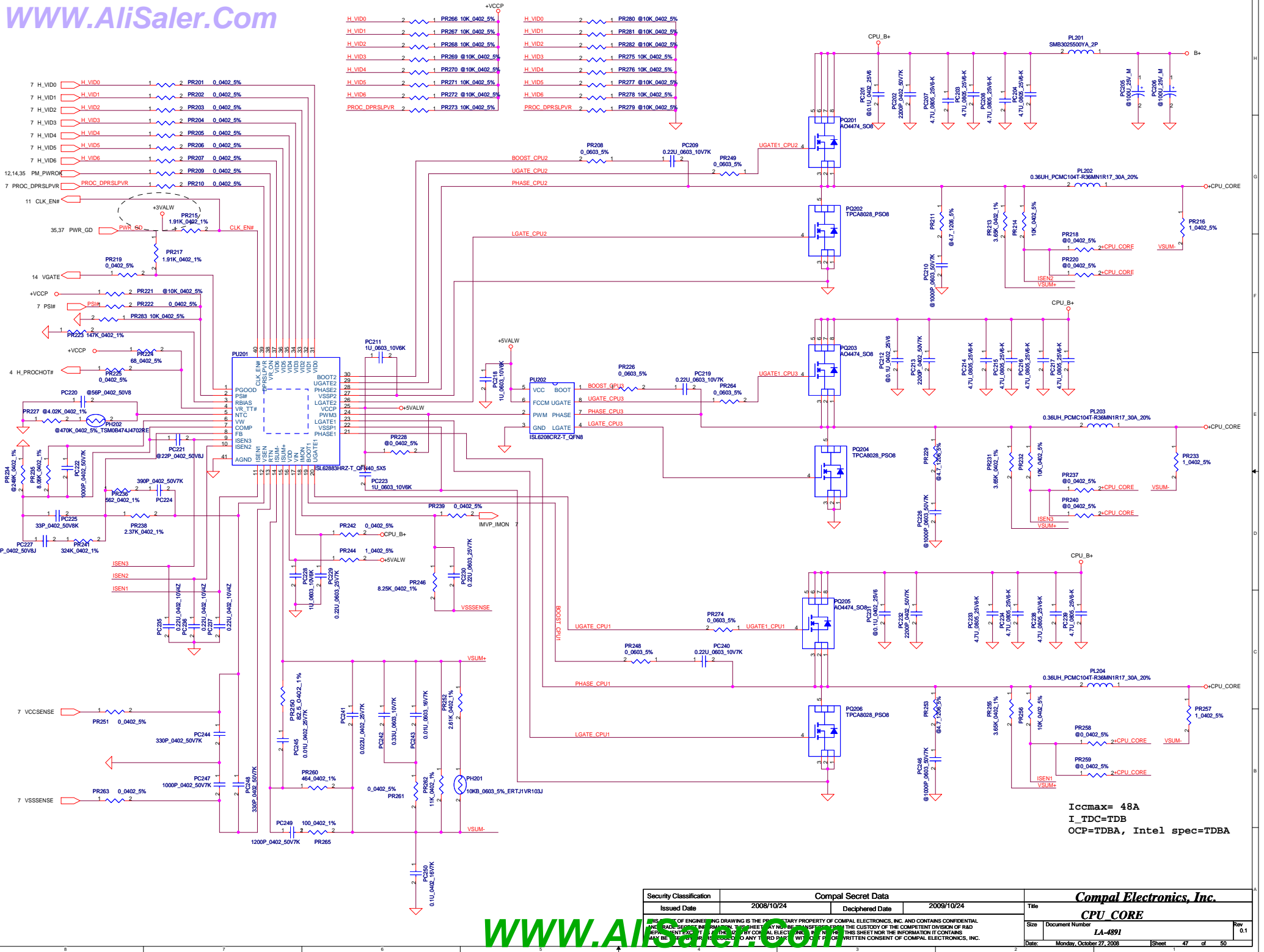
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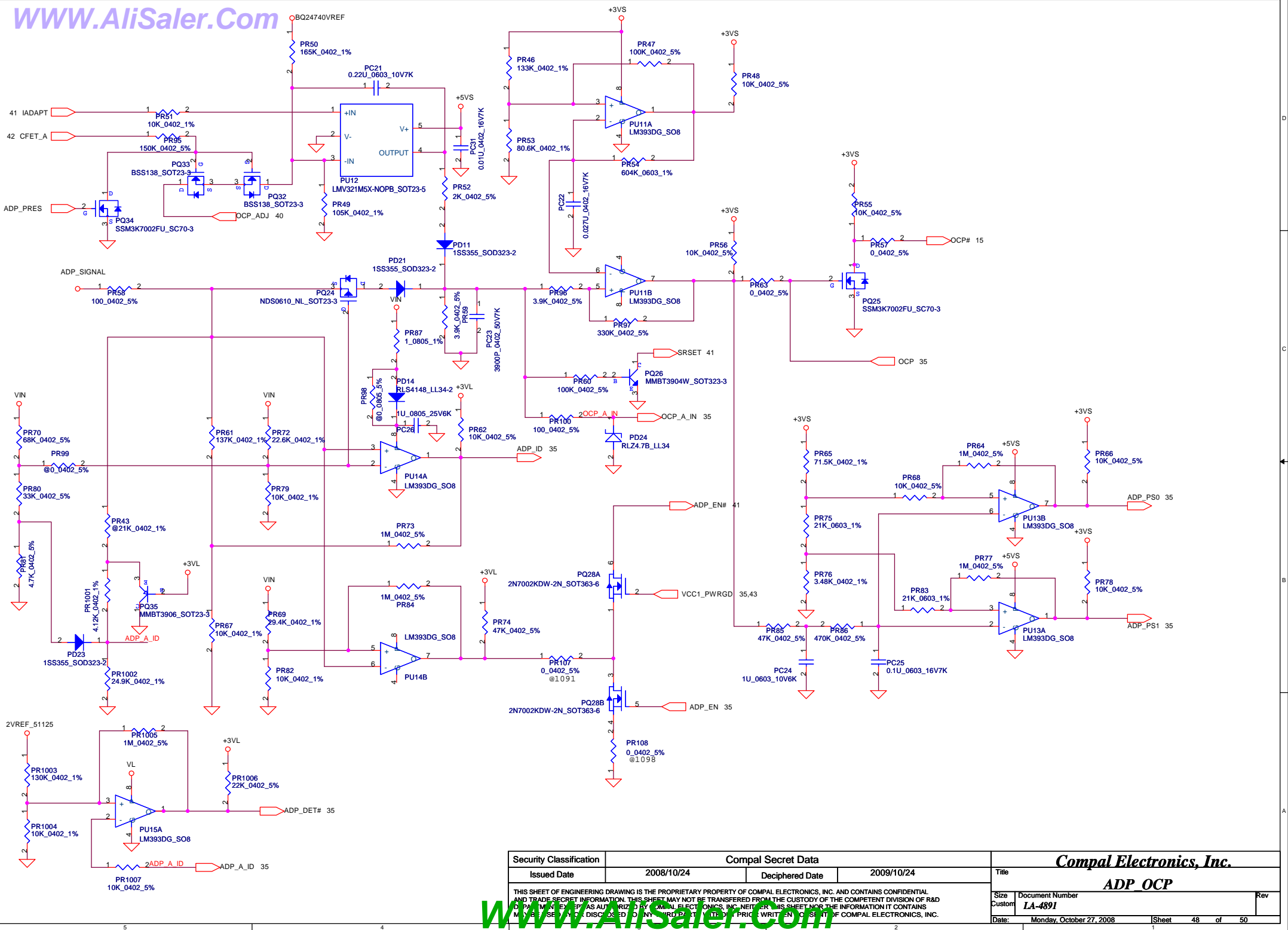


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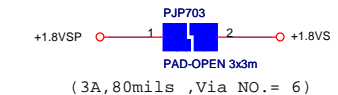


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